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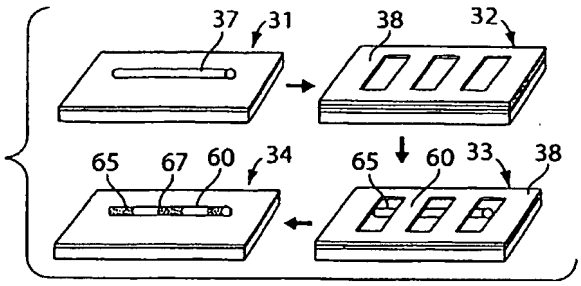
(54) Title: NANOSTRUCTURES CONTAINING METAL-SEMICONDUCTOR COMPOUNDS



(57) Abstract: The present invention generally relates to devices and components for use in nanotechnology and sub-microelectronic circuitry that include metal-semiconductor compounds such as metal silicides. The present invention also, in some embodiments, provides methods of forming such devices and components by allowing a first material to diffuse into a second material, optionally creating a new compound. Thus, as an example, metal atoms are allowed to diffuse into a semiconductor to create the metal-semiconductor compound. In some cases, the device may include a component that is a single crystal. Certain metal-semiconductor compounds of the invention have novel physical/electrical properties, for example, low resistivities, high conductivities, high current density capacities, and the like. In some embodiments, a component of the invention may have two or more regions that differ in composition, where one or both of the regions can include a metal-semiconductor compound. In some cases, the regions may be created by using a mask or a nanoscale wire to define the two or more regions.

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of the dielectric (e.g., by choosing a particular dielectric material), increasing the electrode surface areas (e.g., by making the electrode plates larger, etc.), decreasing the distance between the electrodes, or combinations thereof. As described below, a number of traditional capacitors (e.g., electrolytic capacitors) optimize capacitance by etching/roughening the surface of the electrode to increase the surface area "A."

[0026] It will be appreciated that choice of dielectric material is an effective means of manipulating the qualities of capacitors. For example, metal oxides can be used as materials for dielectrics. In other words, specific oxides are based upon the composition of the electrode plates in the capacitor, e.g., aluminum oxides as dielectrics upon aluminum electrode plates, etc. In many capacitors, aluminum oxide and tantalum oxide (typically tantalum pentoxide) are often chosen. Thus, in many types of capacitors (typically electrolytic capacitors) different metals (e.g., tantalum, aluminum, zinc, niobium and zirconium) are coated with an oxide through an electrochemical process. For example, a thin layer or coating of Al_2O_3 (aluminum oxide) can be formed on an aluminum electrode plate by placing the metal in the proper chemical solution and running an electric current through it. The thickness of such oxide layers (e.g., less than a micrometer, etc.) can be manipulated through changes in reaction conditions. The oxide layer thus formed, comprises the dielectric of the capacitor. Typical dielectrics made of metal oxides can be quite effective in capacitors, and can withstand extremely high fields without breakdown. Various arrangements of such capacitors can be rectifying (typical) or non-rectifying (often constructed with two opposing layers of oxidized material).

[0027] As an often related point, the thickness of the dielectric, which also influences the capacitance, *see* Equation 1, can depend upon the choice of material for the dielectric. For example, oxide layers (e.g., metal oxide layers as described above) are quite thin. Those of skill in the art will be familiar with such thin oxide layers, e.g., from usage in electrolytic capacitors, etc. Such thinness also increases the capacitance in addition to the dielectric constant component/influence of the dielectric material itself because the thinness/thickness of the dielectric is often the distance, or is effectively the distance, between the electrode plates.

[0028] Yet another method of modifying capacitance is through change of the effective areas of the electrode plates. Those of skill in the art will be quite familiar with various means used to increase such effective areas. For example, some capacitors have

increased the surface area of one or both of the electrode plates through, e.g., constructing the electrode plates from activated carbon fibers, etching or sintering of the surfaces of the electrode plates (e.g., etching metal), etc. For example, etching (e.g., chemical etching with acids) can produce an increased surface area 30-100 times greater than an unetched surface. A dielectric (e.g., a metal oxide) is then typically formed/placed over the increased surface area. Those of skill in the art will be knowledgeable about such practices and their corresponding use in construction of capacitors.

[0029] Once the surface area electrode has been covered with a dielectric, the opposing electrode can touch, or effectively touch, the dielectric. For example, a wet electrolytic solution can exist between the dielectric (touching and filling the surface variations) and the opposing electrode. Dry electrolytic material can also fulfill a similar role. In either case, the solutions between the dielectric and the opposing electrode, in effect, become extensions/part of the opposing electrode.

Nanofiber-enhanced Capacitors

[0030] The capacitors of the present invention provide large capacitance values per footprint area of electrode plate, thus, allowing construction of quite small and/or quite powerful capacitors. The capacitors herein have one or more electrode plate which comprises nanofiber surfaces. As explained below, such nanofiber surfaces can optionally encompass myriad nanostructures (e.g., nanowires, nanorods, nanocrystals, etc.) which vastly increase the surface area of the electrode plates. As explained above, increasing the surface area of the electrodes in a capacitor increases its capacitance.

[0031] Figure 2 displays a schematic diagram illustrating one possible embodiment of the current invention. As seen in Figure 2, an electrode plate, 200, comprises a number of nanofibers, 230, upon it. In preferred embodiments, such nanofibers and electrode plate are "coated" with a dielectric, 220, (e.g., typically an oxide layer), which dielectric is then "coated" with another material to form the second, or opposing, electrode plate, 210.

[0032] In typical embodiments, the surface of the electrode plate (e.g., the area between nanofiber attachments) is comprised of a conductive material (e.g., typically a metal, a semiconducting material, an electrically conductive polymer or resin, etc.). Additionally, the nanofibers themselves are preferably comprised of electrically conductive material(s) such as, e.g., metals, semiconducting materials, electrically

conductive polymers, resins, etc. The electrode plate surface and/or the nanofibers on the plate are optionally comprised of silicon or silicon compounds. No matter the exact composition of the nanofibers and the rest of the body of the electrode plate, such features (i.e., the nanofibers and the plate surface) can optionally be comprised of the same material or can optionally be comprised of different materials. For example, the nanofibers can optionally comprise silicon/silicon compounds while the electrode plate can optionally comprise an electrically conductive metal. The possible difference in composition between the nanofibers and the plate surface can arise, e.g., because the plurality of nanofibers can optionally be grown upon a different surface, harvested, and then deposited/attached to the electrode plate surface.

[0033] Also, as can be seen in Figure 2, capacitors of the invention comprise a dielectric that typically "coats" the nanofiber surface of the electrode plate. Thus, the dielectric closely conforms to the shape of the nanofibers and the electrode plate, in effect, forming a coating over them. The dielectric typically coats or covers substantially all nanofibers and/or all areas of the electrode plate which comprises the nanofibers.

[0034] In many embodiments, the dielectric comprises an oxide layer, typically an oxide of the material(s) which form the nanofibers/electrode plate. For example, in some embodiments herein the dielectric comprises a silicon oxide layer coating the nanofibers/electrode plate. In yet other embodiments, the dielectric is one or more of: an oxide, a nitride, a polymer, a ceramic, a resin, a porcelain, a mica containing material, a glass, vacuum, a rare earth oxide, a gas, etc. Those of skill in the art will be familiar with other typical dielectrics used in electronic capacitors and which are capable of use in the present invention. In any case, as with typical capacitors, the dielectric in the present invention consists of a nonconductive material.

[0035] In embodiments wherein the dielectric comprises an oxide layer, such layer can be, e.g., a grown oxide layer or a naturally occurring oxide layer. Again, typical oxide layers herein comprise silicon oxides. Those of skill in the art will also be aware of methods of manipulating thickness and other growth/construction aspects of such oxide layers in order to achieve the desired dielectric parameters. For example, particular environmental conditions present during the growth/construction of oxide layers can influence the thickness of the oxide layer, etc.

[0036] In various embodiments, the dielectric (e.g., the oxide layer) comprises a thickness of from about 1 nm or less to about 1 um, from about 2 nm or less to about 750 nm, from about 5 nm or less to about 500 nm, from about 10 nm or less to about 250 nm, or from about 50 nm or less to about 100 um. In yet other embodiments, the thickness is substantially equivalent to the thickness of the electrode surface comprising the nanofibers.

[0037] In typical embodiments herein, the capacitor comprises a second electrode plate, i.e., an opposing electrode plate that is on the opposite side of the dielectric than the electrode plate comprising the nanofiber surface. In preferred embodiments, this second electrode plate comprises a layer of material deposed upon the dielectric (i.e., covering the plurality of nanofibers on the first electrode plate). *See*, e.g., Figure 2. As with typical capacitors, the second electrode plate is also electrically conductive, e.g., is composed of electrically conductive material(s) such as metals, semiconducting materials, conductive polymers, conductive resins, etc. In order to achieve the close mating between the second electrode plate and the complex nanofiber surface (i.e., coated with the dielectric), the second electrode plate is preferably evaporated or sputtered onto the dielectric. For example, an electrically conductive metal (e.g., aluminum, tantalum, platinum, titanium, nickel, gold, etc.), a semiconducting material, polysilicon, titanium oxide, or an electrolyte, etc. can be used as the material of the second electrode plate. In some embodiments, the second electrode plate can optionally comprise an electrolytic solution (either liquid or non-liquid) which, in effect, acts as the second electrode plate. Those of skill in the art will be familiar with similar electrolytic set-ups from traditional electrolytic capacitors, etc.

[0038] In the various embodiments herein, the capacitors (i.e., the electrode plates comprising the nanofiber surfaces) can have various densities of nanofibers within footprint areas. For example, some embodiments comprise nanofiber densities of from about 0.11 nanofiber per square micron or less to at least about 1000 nanofibers per square micron, from about 1 nanofiber per square micron or less to at least about 500 nanofibers per square micron, from about 10 nanofibers per square micron or less to at least about 250 nanofibers per square micron, or from about 50 nanofibers per square micron or less to at least about 100 nanofibers per square micron.

[0039] Also, in different embodiments herein, the length of the nanofibers within the capacitors can be of different lengths. For example, the length of the nanofibers herein can range from about 1 micron or less to at least about 500 microns, from about 5 micron or less to at least about 150 microns, from about 10 micron or less to at least about 125 microns, or from about 50 micron or less to at least about 100 microns. Also, such various embodiments can comprise nanofibers of various diameters as well. Thus, different embodiments can comprise nanofibers that range in diameter from about 5 nm or less to at least about 1 micron, from about 10 nm or less to at least about 500 nm, from about 20 nm or less to at least about 250 nm, from about 20 nm or less to at least about 200 nm, from about 40 nm or less to at least about 200 nm, from about 50 nm or less to at least about 150 nm, or from about 75 nm or less to at least about 100 nm.

[0040] In the capacitors herein, the addition of the nanofibers to the electrode surface can increase the surface area of the electrode surface (in comparison to an electrode surface which does not have nanofibers) by at least 1.5 times to at least 100,00 times or more, by at least 5 times to at least 75, 000 times or more, by at least 10 times to at least 50,000 times or more, by at least 50 times to at least 25,000 times or more, by at least 100 times to at least 10,000 times or more, or by at least 500 times to at least 1,000 times or more. Such comparisons are typically made by comparing similar "footprints" of electrode plates, i.e., similar or substantially similar area outlines.

[0041] An example of the increase in effective area of an electrode plate of the invention can be seen in Figure 4. The graph in Figure 4 compares the surface area of a nanofiber enhanced area against the distance between the nanofibers on the area. Thus, 10 nm nanowires with a 2 nm aluminum/aluminum oxide coating that are stacked 10 nm apart would produce a surface area that would be ten times greater than any surface reported in the literature.

[0042] Also, within the capacitors herein, addition of nanofibers to the electrode surface/plate can increase the farad capacity of the capacitor by about at least 1.5 times to at least 100,00 times or more, by at least 5 times to at least 75, 000 times or more, by at least 10 times to at least 50,000 times or more, by at least 50 times to at least 25,000 times or more, by at least 100 times to at least 10,000 times or more, or by at least 500 times to at least 1,000 times or more in relation to a capacitor which does not comprise a nanofiber

enhanced surface. Again, such comparisons are typically made against similar or substantially similar footprint or outline areas.

[0043] The current invention also includes devices comprising capacitors with nanofiber enhanced surfaces (i.e., typically nanofiber enhanced electrode plates). Myriad examples of such devices can be contemplated. Those of skill in the art will appreciate the wide range of devices capable of comprising/utilizing these capacitors. Basically, any device requiring a capacitor (especially a capacitor of large farad capability and small size) can comprise/utilize the current invention. Nonlimiting examples of such devices can include, e.g., timepieces, watches, radios, remote controls, nanodevices, medical implant devices (e.g., pacemakers, prosthetic devices with electrical components, etc.), flow through capacitors, e.g., for water purification or solute sorting/separation.

Characteristics of Nanofiber Surface Substrates

[0044] As noted previously, increased surface area is a property that is sought after in many fields (e.g., in substrates for assays or separation column matrices) as well as the current capacitors. For example, fields such as tribology and those involving separations and adsorbents are quite concerned with maximizing surface areas. Other inventions by the inventor and coworkers have focused on such applications. *See*, e.g., NANOFIBER SURFACES FOR USE IN ENHANCED SURFACE AREA APPLICATIONS, USSN 10/792,402, filed March 2, 2004. The current invention offers capacitors, and applications of such, having surfaces that are increased or enhanced with nanofibers (i.e., increased or enhanced in area in relation to structures or surfaces without nanofibers, such as "planar" surfaces).

[0045] A "nanofiber enhanced surface area" or a capacitor or capacitor electrode surface with an "enhanced surface area," etc. herein corresponds to a capacitor or capacitor electrode surface comprising a plurality of nanofibers (e.g., nanowires, nanotubes, nanospheres, etc.) attached to a substrate so that the surface area within a certain "footprint" of the substrate is increased relative to the surface area within the same footprint without the nanofibers. Such footprint corresponds to outlining the parameters of the measurement area.

[0046] As explained in greater detail below, in typical embodiments herein, the nanofibers (and often the electrode surface substrate) are composed of silicon and/or

silicon oxides. It will be noted that such compositions convey a number of benefits in certain embodiments herein. Also, in some embodiments herein, one or more of the plurality of nanofibers is functionalized with one or more moiety. *See*, below. However, it should also be noted that the current invention is not specifically limited by the composition of the nanofibers or of the substrate or of any functionalization, unless otherwise noted.

[0047] Thus, as an illustrative, but not limiting, example, Figures 2 and 3 present schematic and actual representations of nanofiber enhanced surface area substrates of the invention, such as would be constructed within capacitors herein. Figure 2 shows a schematic of a nanofiber capacitor. Figure 3 displays photomicrographs of an enhanced surface area nanofiber substrate such as would form the basis for a nanofiber plate element. It will be noted that the number and shape and distribution of the nanofibers allows ample opportunity for increased surface area, etc. Again, it is to be emphasized that such examples are merely to illustrate the myriad possible embodiments of the current invention.

[0048] The various embodiments of the current invention are adaptable to, and useful for, a great number of different applications. For example, as explained in more detail below, various permutations of the invention can be used in, e.g., any number of devices requiring capacitors. Other uses and embodiments are examined herein.

[0049] As will be appreciated by those of skill in the art, in numerous materials the surface properties can optionally provide a great deal of the functionality or use of the material. For example, in various embodiments, the adherence or coverage of the dielectric is provided by or aided by interaction of the nanofiber elements with appropriate functionalization moieties.

[0050] As also will be appreciated by those of skill in the art, many aspects of the current invention are optionally variable (e.g., surface chemistries on the nanofibers, surface chemistries on any end of the nanofibers or on the substrate surface, etc.). Specific illustration of various modifications, etc. herein, should therefore not be taken as necessarily limiting the current invention. Also, it will be appreciated, and is explained in more detail below, that the length to thickness ratio of the nanofibers herein is optionally varied, as is, e.g., the composition of the nanofibers and the dielectric. Furthermore, a variety of methods can be employed to bring the fibers in contact with surfaces.

Additionally, while some embodiments herein comprise nanofibers that are specifically functionalized in one or more ways, e.g., through attachment of moieties or functional groups to the nanofibers, other embodiments comprise nanofibers which are not functionalized.

Nanofibers and nanofiber construction

[0051] In typical embodiments herein the surfaces (i.e., the nanofiber enhanced area surfaces) and the nanofibers themselves can optionally comprise any number of materials. The actual composition of the surfaces and the nanofibers is based upon a number of possible factors. Such factors can include, for example, the intended use of the enhanced area surfaces, e.g., the specific parameters such as amount of capacitance and/or capacitance per unit area needed, the conditions under which they will be used (e.g., temperature, pH, presence of light (e.g., UV), atmosphere, etc.), the durability of the surfaces and the cost, etc. In typical and preferred embodiments the nanofibers are electrically conductive. The ductility and breaking strength of nanowires will vary depending on, e.g., their composition. For example, ceramic ZnO wires can be more brittle than silicon or glass nanowires, while carbon nanotubes may have a higher tensile strength.

[0052] As explained more fully below, some possible materials used to construct the nanofibers and nanofiber enhanced surfaces herein, include, e.g., silicon, ZnO, TiO, carbon, and carbon nanotubes. *See* below. The nanofibers of the invention are also optionally coated or functionalized, e.g., to enhance or add specific properties. For example, polymers, ceramics or small molecules can optionally be used as coating materials on the nanofibers, e.g., between the nanofibers and the dielectric, etc. The optional coatings can impart characteristics such as water resistance, improved electrical properties, etc. Additionally, specific moieties or functional groups can also be attached to or associated with the nanofibers herein.

[0053] Of course, it will be appreciated that the current invention is not limited by recitation of particular nanofiber and/or substrate compositions, and that, unless otherwise stated, any of a number of other materials are optionally used in different embodiments herein. Additionally, the materials used to comprise the nanofibers can optionally be the

same as the material used to comprise the substrate surfaces or they can be different from the materials used to construct the substrate surfaces.

[0054] In yet other embodiments herein, the nanofibers involved can optionally comprise various physical conformations such as, e.g., nanotubules (e.g., hollow-cored structures), nanorods, nanocrystals, nanowhiskers etc. A variety of nanofiber types are optionally used in this invention including carbon nanotubes, metallic nanotubes, metals and ceramics. Such nanostructures are all optionally used in increasing the surface area of the electrode surfaces, etc. While typical embodiments herein recite "nanofiber," such language should not be construed as necessarily limiting unless specified to be so.

[0055] It is to be understood that this invention is not limited to particular configurations, which can, of course, vary (e.g., different combinations of nanofibers and substrates and optional moieties, etc. which are optionally present in a range of lengths, densities, etc.). It is also to be understood that the terminology used herein is for the purpose of describing particular embodiments only, and is not intended to be necessarily limiting. As used in this specification and the appended claims, the singular forms "a," "an" and "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a nanofiber" optionally includes a plurality of such nanofibers, and the like. Unless defined otherwise, all scientific and technical terms are understood to have the same meaning as commonly used in the art to which they pertain. For the purpose of the present invention, additional specific terms are defined throughout.

A) Nanofibers

[0056] The term "nanofiber" as used herein, refers to a nanostructure typically characterized by at least one physical dimension less than about 1000 nm, less than about 500 nm, less than about 250 nm, less than about 150 nm, less than about 100 nm, less than about 50 nm, less than about 25 nm or even less than about 10 nm or 5 nm. In many cases, the region or characteristic dimension will be along the smallest axis of the structure.

[0057] Nanofibers of this invention typically have one principle axis that is longer than the other two principle axes and, thus, have an aspect ratio greater than one, an aspect ratio of 2 or greater, an aspect ratio greater than about 10, an aspect ratio greater than about 20, or an aspect ratio greater than about 100, 200, or 500. In certain embodiments,

nanofibers herein have a substantially uniform diameter. In some embodiments, the diameter shows a variance less than about 20%, less than about 10%, less than about 5%, or less than about 1% over the region of greatest variability and over a linear dimension of at least 5 nm, at least 10 nm, at least 20 nm, or at least 50 nm. For example, a wide range of diameters could be desirable due to cost considerations and/or to create a more random surface. Typically the diameter is evaluated away from the ends of the nanofiber (*e.g.* over the central 20%, 40%, 50%, or 80% of the nanofiber). In yet other embodiments, the nanofibers herein have a non-uniform diameter (i.e., they vary in diameter along their length). Also in certain embodiments, the nanofibers of this invention are substantially crystalline and/or substantially monocrystalline.

[0058] Once again, it will be appreciated that the term nanofiber, can optionally include such structures as, e.g., nanowires, nanowhiskers, semi-conducting nanofibers, carbon nanotubes or nanotubules and the like.

[0059] The nanofibers of this invention can be substantially homogeneous in material properties, or in certain embodiments they are heterogeneous (e.g. nanofiber heterostructures) and can be fabricated from essentially any convenient material or materials. The nanofibers can comprise "pure" materials, substantially pure materials, doped materials and the like and can include, in various combinations, insulators, conductors, and semiconductors. Additionally, while some illustrative nanofibers herein are comprised of silicon (or silicon oxides), as explained above, they optionally can be comprised of any of a number of different materials, unless otherwise stated.

[0060] Composition of nanofibers can vary depending upon a number of factors, e.g., specific functionalization (if any) to be associated with or attached to the nanofibers, durability, cost, conditions of use, etc. The composition of nanofibers is quite well known to those of skill in the art. As will be appreciated by such skilled persons, the nanofibers of the invention can, thus, be composed of any of a myriad of possible substances (or combinations thereof). Some embodiments herein comprise nanofibers composed of one or more organic or inorganic compound or material. Any recitation of specific nanofiber compositions herein should not be taken as necessarily limiting.

[0061] Additionally, the nanofibers of the invention are optionally constructed through any of a number of different methods, and examples listed herein should not be taken as necessarily limiting. Thus, nanofibers constructed through means not specifically

described herein, but which fall within the parameters as set forth herein are still nanofibers of the invention and/or are used with the devices and methods of the invention.

[0062] In a general sense, the nanofibers of the current invention often (but not exclusively) comprise long thin protuberances (e.g., fibers, nanowires, nanotubules, etc.) grown from a solid, optionally planar, substrate. Of course, in some embodiments herein, the fibers are detached from the substrate on which they are grown and attached to a second substrate. The second substrate need not be planar and, in fact, can comprise a myriad of three-dimensional conformations, as can the substrate on which the nanofibers were grown originally. In some embodiments herein, the substrates are flexible. Also, as explained in greater detail below, nanofibers of the invention can be grown/constructed in, or upon, variously configured surfaces, e.g., on a flat substrate that is rolled into an overlapping cylinder, etc. *See infra.*

[0063] In various embodiments herein, the nanofibers involved are optionally grown on a first substrate and then subsequently transferred to a second substrate which is to have the enhanced surface area. Such embodiments are particularly useful in situations wherein the substrate desired needs to be flexible or conforming to a particular three dimensional shape that is not readily subjected to direct application or growth of nanofibers thereon. For example, nanofibers can be grown on such rigid surfaces as, e.g., silicon wafers or other similar substrates. The nanofibers thus grown can then optionally be transferred to a flexible backing. Again, it will be appreciated, however, that the invention is not limited to particular nanofiber or substrate compositions. For example, nanofibers are optionally gown on any of a variety of different surfaces, including, e.g., flexible foils such as aluminum or the like. Additionally, for high temperature growth processes, any metal, ceramic or other thermally stable material is optionally used as a substrate on which to grow nanofibers of the invention. Furthermore, low temperature synthesis methods such as solution phase methods can be utilized in conjunction with an even wider variety of substrates on which to grow nanofibers. For example, flexible polymer substrates and other similar substances are optionally used as substrates for nanofiber growth/attachment.

[0064] As one example, the growth of nanofibers on a surface using a gold catalyst has been demonstrated in the literature. Applications targeted for such fibers are based on harvesting them from the substrate and then assembling them into devices. However, in

many other embodiments herein, the nanofibers involved in enhanced surface areas are grown in place. Available methods, such as growing nanofibers from gold colloids deposited on surfaces are, thus, optionally used herein. The end product which results is the substrate upon which the fibers are grown (i.e., with an enhanced surface area due to the nanofibers). As will be appreciated, specific embodiments and uses herein, unless stated otherwise, can optionally comprise nanofibers grown in the place of their use and/or through nanofibers grown elsewhere, which are harvested and transferred to the place of their use. For example, many embodiments herein relate to leaving the fibers intact on the growth substrate and taking advantage of the unique properties the fibers impart on the substrate. Other embodiments relate to growth of fibers on a first substrate and transfer of the fibers to a second substrate to take advantage of the unique properties that the fibers impart on the second substrate.

[0065] For example, if nanofibers of the invention were grown on, e.g., a non-flexible substrate (e.g., such as some types of silicon wafers) they could be transferred from such non-flexible substrate to a flexible substrate (e.g., such as a conductive flexible metallic material). Again, as will be apparent to those of skill in the art, the nanofibers herein could optionally be grown on a flexible substrate to start with, but different desired parameters may influence such decisions.

[0066] A variety of methods may be employed in transferring nanofibers from a surface upon which they are fabricated to another surface. For example, nanofibers may be harvested into a liquid suspension, e.g., ethanol, which is then coated onto another surface. Additionally, nanofibers from a first surface (e.g., ones grown on the first surface or which have been transferred to the first surface) can optionally be "harvested" by applying a sticky coating or material to the nanofibers and then peeling such coating/material away from the first surface. The sticky coating/material is then optionally placed against a second surface to deposit the nanofibers. Examples of sticky coatings/materials which are optionally used for such transfer include, but are not limited to, e.g., tape (e.g., 3M Scotch® tape), magnetic strips, curing adhesives (e.g., epoxies, rubber cement, etc.), etc. The nanofibers could be removed from the growth substrate, mixed into a plastic, and then surface of such plastic could be ablated or etched away to expose the fibers.

[0067] The actual nanofiber constructions of the invention are optionally complex. For example, Figure 3 is a photomicrograph of a typical nanofiber construction. As can be seen in Figure 3, the nanofibers form a complex three-dimensional pattern. Possible interlacing and variable heights, curves, bends, etc. can form a surface which greatly increases the surface area per unit substrate (e.g., as compared with a planar surface without nanofibers). Of course, in other embodiments herein, it should be apparent that the nanofibers need not be as complex as, e.g., those shown in Figure 3. Thus, in many embodiments herein, the nanofibers are "straight" and do not tend to bend, curve, or curl. However, such straight nanofibers are still encompassed within the current invention.

B) Functionalization

[0068] Some embodiments of the invention comprise nanofiber and nanofiber enhanced area surfaces in which the fibers include one or more functional moiety (e.g., a chemically reactive group) attached to them. Functionalized nanofibers are optionally used in many different embodiments, e.g., to confer increased electrical conductance to the nanofibers, to help the dielectric adhere/bond to the nanofibers, etc. Beneficially, typical embodiments of enhanced surface areas herein are comprised of silicon oxides, which are conveniently modified with a large variety of moieties. Of course, other embodiments herein are comprised of other nanofiber compositions (e.g., polymers, ceramics, metals that are coated by CVD or sol-gel sputtering, etc.) which are also optionally functionalized for specific purposes. Those of skill in the art will be familiar with numerous functionalizations and functionalization techniques which are optionally used herein.

[0069] Further relevant information can be found in CRC Handbook of Chemistry and Physics (2003) 83rd edition by CRC Press. Details on conductive and other coatings, which can also be incorporated onto nanofibers of the invention by plasma methods and the like can be found in H. S. Nalwa (ed.), Handbook of Organic Conductive Molecules and Polymers, John Wiley & Sons 1997. *See* also, ORGANIC SPECIES THAT FACILITATE CHARGE TRANSFER TO/FROM NANOCRYSTALS USSN 60/452,232 filed March 4, 2003 by Whiteford et al. Additionally, details regarding relevant moiety and other chemistries, as well as methods for construction/use of such, can be found, e.g., in Hermanson Bioconjugate Techniques Academic Press (1996), Kirk-Othmer Concise Encyclopedia of Chemical Technology (1999) Fourth Edition by Grayson et al. (ed.) John Wiley & Sons, Inc., New York and in Kirk-Othmer Encyclopedia of Chemical

Technology Fourth Edition (1998 and 2000) by Grayson et al. (ed.) Wiley Interscience (print edition)/ John Wiley & Sons, Inc. (e-format). Details regarding organic chemistry, relevant for, e.g., coupling of additional moieties to a functionalized surface of nanofibers can be found, e.g., in Greene (1981) Protective Groups in Organic Synthesis, John Wiley and Sons, New York, as well as in Schmidt (1996) Organic Chemistry Mosby, St Louis, MO, and March's Advanced Organic Chemistry Reactions, Mechanisms and Structure, Fifth Edition (2000) Smith and March, Wiley Interscience New York ISBN 0-471-58589-0. Those of skill in the art will be familiar with many other related references and techniques amenable for functionalization of the nanofibers herein.

[0070] Thus, again as will be appreciated, the substrates involved, the nanofibers involved (e.g., attached to, or deposited upon, the substrates), and any optional functionalization of the nanofibers and/or substrates, and the like can be varied. For example, the length, diameter, conformation and density of the fibers can be varied, as can the composition of the fibers and their surface chemistry.

C) Density and Related Issues

[0071] In terms of density, it will be appreciated that by including more nanofibers emanating from a surface, one automatically increases the amount of surface area that is extended from the basic underlying substrate. This, thus, increases the amount of intimate contact area between the surface and the dielectric and, indirectly, to the opposing electrode plate coming into contact with the nanofiber surfaces. As explained in more detail below, the embodiments herein optionally comprise a density of nanofibers on a surface of from about 0.1 to about 1000 or more nanofibers per micrometer^2 of the substrate surface. Again, here too, it will be appreciated that such density depends upon factors such as the diameter of the individual nanofibers, etc. *See*, below. The nanofiber density influences the enhanced surface area, since a greater number of nanofibers will tend to increase the overall amount of area of the surface. Therefore, the density of the nanofibers herein typically has a bearing on the increased capacitance of the enhanced surface area materials because such density is a factor in the overall area of the surface.

[0072] For example, a typical flat planar substrate, e.g., a silicon oxide chip or a glass slide, will typically comprise "x" surface area per square micron (i.e., within a square micron footprint). However, if such a substrate surface were coated with

nanofibers, then the available surface area would be much greater. In some embodiments herein each nanofiber on a surface comprises about 1 square micron in surface area (i.e., the sides and tip of each nanofiber present that much surface area). If a comparable square micron of substrate comprised from 10 to about 100 nanofibers per square micron, the available surface area is thus 10 to 100 times greater than a plain flat surface. Therefore, in the current illustration, an enhanced surface area would have 10x to 100x more surface area per square micron footprint. It will be appreciated that the density of nanofibers on a substrate is influenced by, e.g., the diameter of the nanofibers and any functionalization of such fibers, etc.

[0073] Different embodiments of the invention comprise a range of such different densities (i.e., number of nanofibers per unit area of a substrate to which nanofibers are attached). The number of nanofibers per unit area can optionally range from about 1 nanofiber per 10 micron^2 up to about 200 or more nanofibers per micron^2; from about 1 nanofiber per micron^2 up to about 150 or more nanofibers per micron^2; from about 10 nanofibers per micron^2 up to about 100 or more nanofibers per micron^2; or from about 25 nanofibers per micron^2 up to about 75 or more nanofibers per micron^2. In yet other embodiments, the density can optionally range from about 1 to 3 nanowires per square micron to up to approximately 2,500 or more nanowires per square micron.

[0074] In terms of individual fiber dimensions, it will be appreciated that by increasing the thickness or diameter of each individual fiber one will, again, automatically increase the overall area of the fiber and, thus, the overall area of the substrate and, hence, the electrode plate. The diameter of nanofibers herein can be controlled through, e.g., choice of compositions and growth conditions of the nanofibers, addition of moieties, coatings or the like, etc. Preferred fiber thicknesses are optionally between from about 5 nm up to about 1 micron or more (e.g., 5 microns); from about 10 nm to about 750 nanometers or more; from about 25 nm to about 500 nanometers or more; from about 50 nm to about 250 nanometers or more, or from about 75 nm to about 100 nanometers or more. In some embodiments, the nanofibers comprise a diameter of approximately 40 nm.

[0075] In addition to diameter, surface area of nanofibers (and therefore surface area of a substrate to which the nanofibers are attached and, thus, of the electrode plate) also is influenced by length of the nanofibers. Of course, it will also be understood that for some fiber materials, increasing length may yield increasing fragility. Accordingly,

preferred fiber lengths will typically be between about 2 microns (e.g., 0.5 microns) up to about 1 mm or more; from about 10 microns to about 500 micrometers or more; from about 25 microns to about 250 microns or more; or from about 50 microns to about 100 microns or more. Some embodiments comprise nanofibers of approximately 50 microns in length. Some embodiments herein comprise nanofibers of approximately 40 nm in diameter and approximately 50 microns in length.

[0076] Nanofibers herein can present a variety of aspect ratios. Thus, nanofiber diameter can comprise, e.g., from about 5 nm up to about 1 micron or more (e.g., 5 microns); from about 10 nm to about 750 nanometers or more; from about 25 nm to about 500 nanometers or more; from about 50 nm to about 250 nanometers or more, or from about 75 nm to about 100 nanometers or more, while the lengths of such nanofibers can comprise, e.g., from about 2 microns (e.g., 0.5 microns) up to about 1 mm or more; from about 10 microns to about 500 micrometers or more; from about 25 microns to about 250 microns or more; or from about 50 microns to about 100 microns or more

[0077] Fibers that are, at least in part, elevated above a surface are particularly preferred, e.g., where at least a portion of the fibers in the fiber surface are elevated at least 10 nm, or even at least 100 nm above a surface, in order to provide enhanced surface area available for coating with a dielectric and the opposing electrode plate.

[0078] Again, as seen in Figure 3, the nanofibers optionally form a complex three-dimensional structure. The degree of such complexity depends in part upon, e.g., the length of the nanofibers, the diameter of the nanofibers, the length:diameter aspect ratio of the nanofibers, moieties (if any) attached to the nanofibers, and the growth conditions of the nanofibers, etc. The bending, interlacing, etc. of nanofibers, which help affect the degree of enhanced surface area available, are optionally manipulated through, e.g., control of the number of nanofibers per unit area as well as through the diameter of the nanofibers, the length and the composition of the nanofibers, etc. Thus, it will be appreciated that enhanced surface area of nanofiber substrates herein is optionally controlled through manipulation of these and other parameters.

[0079] Also, in some, but not all, embodiments herein, the nanofibers of the invention comprise bent, curved, or even curled forms. As can be appreciated, if a single nanofiber snakes or coils over a surface (but is still just a single fiber per unit area bound to a first surface), the fiber can still provide an enhanced surface area due to its length, etc.

D) Nanofiber Construction

[0080] As will be appreciated, the current invention is not limited by the means of construction of the nanofibers herein. For example, while some of the nanofibers herein are composed of silicon, the use of silicon should not be construed as necessarily limiting. For example, a number of other electrically conductive materials are optionally used. The formation of nanofibers is possible through a number of different approaches that are well known to those of skill in the art, all of which are amenable to embodiments of the current invention.

[0081] Typical embodiments herein can be used with existing methods of nanostructure fabrication, as will be known by those skilled in the art, as well as methods mentioned or described herein. In other words, a variety of methods for making nanofibers and nanofiber containing structures have been described and can be adapted for use in various embodiments of the invention.

[0082] The nanofibers can be fabricated of essentially any convenient electrically conductive material (e.g., a semiconducting material, a ferroelectric material, a metal, ceramic, polymers, etc.) and can comprise essentially a single material or can be heterostructures. For example, the nanofibers can comprise a semiconducting material, for example a material comprising a first element selected from group 2 or from group 12 of the periodic table and a second element selected from group 16 (e.g., ZnS, ZnO, ZnSe, ZnTe, CdS, CdSe, CdTe, HgS, HgSe, HgTe, MgS, MgSe, MgTe, CaS, CaSe, CaTe, SrS, SrSe, SrTe, BaS, BaSe, BaTe, and like materials); a material comprising a first element selected from group 13 and a second element selected from group 15 (e.g., GaN, GaP, GaAs, GaSb, InN, InP, InAs, InSb, and like materials); a material comprising a group 14 element (Ge, Si, and like materials); a material such as PbS, PbSe, PbTe, AlS, AlP, and AlSb; or an alloy or a mixture thereof.

[0083] In some embodiments herein, the nanofibers are optionally comprised of silicon or a silicon oxide. It will be understood by one of skill in the art that the term "silicon oxide" as used herein can be understood to refer to silicon at any level of oxidation. Thus, the term silicon oxide can refer to the chemical structure SiO_x, wherein x is between 0 and 2 inclusive. In other embodiments, the nanofibers can comprise, e.g., silicon, glass, quartz, plastic, metal, polymers, TiO, ZnO, ZnS, ZnSe, ZnTe, CdS, CdSe, CdTe, HgS, HgSe, HgTe, MgS, MgSe, MgTe, CaS, CaSe, CaTe, SrS, SrSe, SrTe, BaS,

BaSe, BaTe, GaN, GaP, GaAs, GaSb, InN, InP, InAs, InSb, PbS, PbSe, PbTe, AlS, AlP, AlSb, SiO_1, SiO_2, silicon carbide, silicon nitride, polyacrylonitrile (PAN), polyetherketone, polyimide, aromatic polymers, or aliphatic polymers that are electrically conductive.

[0084] It will be appreciated that in some embodiments, the nanofibers can comprise the same material as one or more substrate surface (i.e., a surface to which the nanofibers are attached or associated), while in other embodiments, the nanofibers comprise a different material than the substrate surface. Additionally, the substrate surfaces can optionally comprise any one or more of the same materials or types of materials as do the nanofibers (e.g., such as the materials illustrated herein).

[0085] As previously stated, some, but by no means all, embodiments herein comprise silicon nanofibers. Common methods for making silicon nanofibers include vapor liquid solid growth (VLS), laser ablation (laser catalytic growth) and thermal evaporation. *See*, for example, Morales et al. (1998) "A Laser Ablation Method for the Synthesis of Crystalline Semiconductor Nanowires" Science 279, 208-211 (1998). In one example approach a hybrid pulsed laser ablation/chemical vapor deposition (PLA-CVD) process for the synthesis of semiconductor nanofibers with longitudinally ordered heterostructures, and variations thereof can be used. *See*, Wu et al. (2002) "Block-by-Block Growth of Single-Crystalline Si/SiGe Superlattice Nanowires," Nano Letters Vol. 0, No. 0.

[0086] In general, multiple methods of making nanofibers have been described and can be applied in the embodiments herein. In addition to Morales et al. and Wu et al. (above), *see*, for example, Lieber et al. (2001) "Carbide Nanomaterials" USPN 6,190,634 B1; Lieber et al. (2000) "Nanometer Scale Microscopy Probes" USPN 6,159,742; Lieber et al. (2000) "Method of Producing Metal Oxide Nanorods" USPN 6,036,774; Lieber et al. (1999) "Metal Oxide Nanorods" USPN 5,897,945; Lieber et al. (1999) "Preparation of Carbide Nanorods" USPN 5,997,832; Lieber et al. (1998) "Covalent Carbon Nitride Material Comprising C_2N and Formation Method" USPN 5,840,435; Thess, et al. (1996) "Crystalline Ropes of Metallic Carbon Nanotubes" Science 273:483-486; Lieber et al. (1993) "Method of Making a Superconducting Fullerene Composition By Reacting a Fullerene with an Alloy Containing Alkali Metal" USPN 5,196,396; and Lieber et al. (1993) "Machining Oxide Thin Films with an Atomic Force Microscope: Pattern and

Object Formation on the Nanometer Scale" USPN 5,252,835. One dimensional semiconductor heterostructure nanocrystals, have been described. *See*, e.g., Bjork et al. (2002) "One-dimensional Steeplechase for Electrons Realized" Nano Letters Vol. 0, No. 0.

[0087] It should be noted that some references herein, while not specific to nanofibers, are typically still applicable to the invention. For example, background issues of construction conditions and the like are applicable between nanofibers and other nanostructures (e.g., nanocrystals, etc.). Also, while described generally in terms of nanofibers and the like, again, it will be appreciated that nanospheres, nanocrystals, etc. are also optionally used to increase the surface area and capacitance of the embodiments herein. *See* above.

[0088] In another approach which is optionally used to construct nanofibers of the invention, synthetic procedures to prepare individual nanofibers on surfaces and in bulk are described, for example, by Kong, et al. (1998) "Synthesis of Individual Single-Walled Carbon Nanotubes on Patterned Silicon Wafers," Nature 395:878-881, and Kong, et al. (1998) "Chemical Vapor Deposition of Methane for Single-Walled Carbon Nanotubes," Chem. Phys. Lett. 292:567-574.

[0089] In yet another approach, substrates and self assembling monolayer (SAM) forming materials can be used, e.g., along with microcontact printing techniques to make nanofibers, such as those described by Schon, Meng, and Bao, "Self-assembled monolayer organic field-effect transistors," Nature 413:713 (2001); Zhou et al. (1997) "Nanoscale Metal/Self-Assembled Monolayer/Metal Heterostructures," Applied Physics Letters 71:611; and WO 96/29629 (Whitesides, et al., published June 26, 1996).

[0090] In some embodiments herein, nanofibers can be synthesized using a metallic catalyst. A benefit of such embodiments allows use of unique materials suitable for surface modifications to create enhanced properties. A unique property of such nanofibers is that they are capped at one end with a catalyst, typically gold. This catalyst end can optionally be functionalized using, e.g., thiol chemistry without affecting the rest of the fiber, thus, making it capable of bonding to an appropriate surface. In such embodiments, the result of such functionalization, etc., is to make a surface with end-linked nanofibers. These resulting "fuzzy" surfaces, therefore, have increased surface areas (i.e., in relation to the surfaces without the nanofibers) and other unique properties.

In some such embodiments, the surface of the nanofiber and/or the target substrate surface is optionally chemically modified (typically, but not necessarily, without affecting the gold tip) in order to give a wide range of properties useful in many applications.

[0091] In other embodiments, to increase or enhance a surface area, the nanofibers are optionally laid "flat" (i.e., substantially parallel to the substrate surface) by chemical or electrostatic interaction on surfaces, instead of end-linking the nanofibers to the substrate. In yet other embodiments herein, techniques involve coating the base surface with functional groups which repel the polarity on the nanofiber so that the fibers do not lay on the surface but are end-linked.

[0092] Synthesis of nanostructures, e.g., nanocrystals, of various composition is described in, e.g., Peng et al. (2000) "Shape control of CdSe nanocrystals" Nature 404:59-61; Puntes et al. (2001) "Colloidal nanocrystal shape and size control: The case of cobalt" Science 291:2115-2117; USPN 6,306,736 to Alivisatos et al. (October 23, 2001) entitled "Process for forming shaped group III-V semiconductor nanocrystals, and product formed using process"; USPN 6,225,198 to Alivisatos et al. (May 1, 2001) entitled "Process for forming shaped group II-VI semiconductor nanocrystals, and product formed using process"; USPN 5,505,928 to Alivisatos et al. (April 9, 1996) entitled "Preparation of III-V semiconductor nanocrystals"; USPN 5,751,018 to Alivisatos et al. (May 12, 1998) entitled "Semiconductor nanocrystals covalently bound to solid inorganic surfaces using self-assembled monolayers"; USPN 6,048,616 to Gallagher et al. (April 11, 2000) entitled "Encapsulated quantum sized doped semiconductor particles and method of manufacturing same"; and USPN 5,990,479 to Weiss et al. (November 23, 1999) entitled "Organo luminescent semiconductor nanocrystal probes for biological applications and process for making and using such probes."

[0093] Additional information on growth of nanofibers, such as nanowires, having various aspect ratios, including nanofibers with controlled diameters, is described in, e.g., Gudiksen et al. (2000) "Diameter-selective synthesis of semiconductor nanowires" J. Am. Chem. Soc. 122:8801-8802; Cui et al. (2001) "Diameter-controlled synthesis of single-crystal silicon nanowires" Appl. Phys. Lett. 78:2214-2216; Gudiksen et al. (2001) "Synthetic control of the diameter and length of single crystal semiconductor nanowires" J. Phys. Chem. B 105:4062-4064; Morales et al. (1998) "A laser ablation method for the synthesis of crystalline semiconductor nanowires" Science 279:208-211; Duan et al.

(2000) "General synthesis of compound semiconductor nanowires" Adv. Mater. 12:298-302; Cui et al. (2000) "Doping and electrical transport in silicon nanowires" J. Phys. Chem. B 104:5213-5216; Peng et al. (2000), *supra*; Puntes et al. (2001), *supra*; USPN 6,225,198 to Alivisatos et al., *supra*; USPN 6,036,774 to Lieber et al. (March 14, 2000) entitled "Method of producing metal oxide nanorods"; USPN 5,897,945 to Lieber et al. (April 27, 1999) entitled "Metal oxide nanorods"; USPN 5,997,832 to Lieber et al. (December 7, 1999) "Preparation of carbide nanorods"; Urbau et al. (2002) "Synthesis of single-crystalline perovskite nanowires composed of barium titanate and strontium titanate" J. Am. Chem. Soc., 124:1186; Yun et al. (2002) "Ferroelectric Properties of Individual Barium Titanate Nanowires Investigated by Scanned Probe Microscopy" Nano Letters 2, 447; and published PCT application nos. WO 02/17362, and WO 02/080280.

[0094] Growth of branched nanofibers (e.g., nanotetrapods, tripods, bipods, and branched tetrapods) is described in, e.g., Jun et al. (2001) "Controlled synthesis of multi-armed CdS nanorod architectures using monosurfactant system" J. Am. Chem. Soc. 123:5150-5151; and Manna et al. (2000) "Synthesis of Soluble and Processable Rod-, Arrow-, Teardrop-, and Tetrapod-Shaped CdSe Nanocrystals" J. Am. Chem. Soc. 122:12700-12706. Synthesis of nanoparticles is described in, e.g., USPN 5,690,807 to Clark Jr. et al. (November 25, 1997) entitled "Method for producing semiconductor particles"; USPN 6,136,156 to El-Shall, et al. (October 24, 2000) entitled "Nanoparticles of silicon oxide alloys"; USPN 6,413,489 to Ying et al. (July 2, 2002) entitled "Synthesis of nanometer-sized particles by reverse micelle mediated techniques"; and Liu et al. (2001) "Sol-Gel Synthesis of Free-Standing Ferroelectric Lead Zirconate Titanate Nanoparticles" J. Am. Chem. Soc. 123:4344. Synthesis of nanoparticles is also described in the above citations for growth of nanocrystals, and nanofibers such as nanowires, branched nanowires, etc.

[0095] Synthesis of core-shell nanofibers, e.g., nanostructure heterostructures, is described in, e.g., Peng et al. (1997) "Epitaxial growth of highly luminescent CdSe/CdS core/shell nanocrystals with photostability and electronic accessibility" J. Am. Chem. Soc. 119:7019-7029; Dabbousi et al. (1997) "(CdSe)ZnS core-shell quantum dots: Synthesis and characterization of a size series of highly luminescent nanocrystallites" J. Phys. Chem. B 101:9463-9475; Manna et al. (2002) "Epitaxial growth and photochemical annealing of graded CdS/ZnS shells on colloidal CdSe nanorods" J. Am. Chem. Soc. 124:7136-7145;

and Cao et al. (2000) "Growth and properties of semiconductor core/shell nanocrystals with InAs cores" J. Am. Chem. Soc. 122:9692-9702. Similar approaches can be applied to growth of other core-shell nanostructures. *See*, for example, USPN 6,207,229 (March 27, 2001) and USPN 6,322,901 (November 27, 2001) to Bawendi et al. entitled "Highly luminescent color-selective materials."

[0096] Growth of homogeneous populations of nanofibers, including nanofiber heterostructures in which different materials are distributed at different locations along the long axis of the nanofibers is described in, e.g., published PCT application numbers WO 02/17362, and WO 02/080280; Gudiksen et al. (2002) "Growth of nanowire superlattice structures for nanoscale photonics and electronics" Nature 415:617-620; Bjork et al. (2002) "One-dimensional steeplechase for electrons realized" Nano Letters 2:86-90; Wu et al. (2002) "Block-by-block growth of single-crystalline Si/SiGe superlattice nanowires" Nano Letters 2, 83-86; and US patent application 60/370,095 (April 2, 2002) to Empedocles entitled " Nanowire heterostructures for encoding information." Similar approaches can be applied to growth of other heterostructures and applied to the various devices, methods and systems herein.

[0097] In some embodiments the nanofibers used to create enhanced surface areas can be comprised of nitride (e.g., AlN, GaN, SiN, BN) or carbide (e.g., SiC, TiC, Tungsten carbide, boron carbide) in order to create nanofibers with high strength and durability. Alternatively, such nitrides/carbides are used as hard coatings on lower strength (e.g., silicon or ZnO) nanofibers. While the dimensions of silicon nanofibers are excellent for many applications requiring enhanced surface area (e.g., *see*, throughout and "Structures, Systems and Methods for Joining Articles and Materials and Uses Therefore," filed April 17, 2003, USSN 60/463,766, etc.) other capacitor applications can require nanofibers that are less brittle and which break less easily. Therefore, some embodiments herein take advantage of materials such as nitrides and carbides which have higher bond strengths than, e.g., Si, SiO_2 or ZnO. The nitrides and carbides are optionally used as coatings to strengthen the weaker nanofibers or even as nanofibers themselves.

[0098] Carbides and nitrides can be applied as coatings to low strength fibers by deposition techniques such as sputtering and plasma processes. In some embodiments, to achieve high strength nanocoatings of carbide and nitride coatings, a random grain orientation and/or amorphous phase is grown to avoid crack propagation. Optimum

conformal coating of the nanofibers can optionally be achieved if the fibers are growing perpendicular to a substrate surface. The hard coating for fibers in such orientation also acts to enhance the adhesion of the fibers to the substrate. For fibers that are randomly oriented, the coating is preferential to the upper layer of fibers. Further information on coating nanostructure surfaces (e.g., to deposit a dielectric layer or to construct a second electrode plate) is presented herein.

[0099] Low temperature processes for creation of silicon nanofibers are achieved by the decomposition of silane at about 400°C in the presence of a gold catalyst. However, as previously stated, silicon nanofibers can be too brittle for some applications to form a durable nanofiber matrix (i.e., an enhanced surface area). Thus, formation and use of, e.g., SiN is optionally utilized in some embodiments herein. In those embodiments, NH_3, which has decomposition at about 300°C, is used to combine with silane to form SiN nanofibers (also by using a gold catalyst). Other catalytic surfaces to form such nanofibers can include, e.g., Ti, Fe, etc.

[0100] Forming carbide and nitride nanofibers directly from a melt can sometimes be challenging since the temperature of the liquid phase is typically greater than 1000°C. However, a nanofiber can be grown by combining the metal component with the vapor phase. For example, GaN and SiC nanofibers have been grown (*see*, e.g., Peidong, Lieber, *supra*) by exposing Ga melt to NH_3 (for GaN) and graphite with silane (SiC). Similar concepts are optionally used to form other types of carbide and nitride nanofibers by combing metal-organic vapor species, e.g., tungsten carbolic [W(CO)6] on a carbon surface to form tungsten carbide (WC), or titanium dimethoxy dineodecanoate on a carbon surface to form TiC. It will be appreciated that in such embodiments, the temperature, pressure, power of the sputtering and the CVD process are all optionally varied depending upon, e.g., the specific parameters desired in the end nanofibers. Additionally, several types of metal organic precursors and catalytic surfaces used to form the nanofibers, as well as, the core materials for the nanofibers (e.g., Si, ZnO, etc.) and the substrates containing the nanofibers, are all also variable from one embodiment to another depending upon, e.g., the specific enhanced nanofiber surface area capacitor to be constructed.

[0101] The present invention can be used with structures that may fall outside of the size range of typical nanostructures. For example, Haraguchi et al. (USPN 5,332,910) describes nanowhiskers which are optionally used herein in design and construction of

capacitors. Semi-conductor whiskers are also described by Haraguchi et al. (1994) "Polarization Dependence of Light Emitted from GaAs p-n junctions in quantum wire crystals" J. Appl. Phys. 75(8):4220-4225; Hiruma et al. (1993) "GaAs Free Standing Quantum Sized Wires," J. Appl. Phys. 74(5):3162-3171; Haraguchi et al. (1996) "Self Organized Fabrication of Planar GaAs Nanowhisker Arrays"; and Yazawa (1993) "Semiconductor Nanowhiskers" Adv. Mater. 5(78):577-579. Such nanowhiskers are optionally nanofibers of the invention. While the above references (and other references herein) are optionally used for construction and determination of parameters of nanofibers of the invention, those of skill in the art will be familiar with other methods of nanofiber construction/design, etc. which can also be amenable to the methods and devices herein.

[0102] Some embodiments herein comprise methods for improving the density and control of nanowire growth as is relates to generating a nanostructured surface coating of substrates. Such methods include repetitive cycling of nanofiber synthesis and gold fill deposition to make "nano-trees" as well as the co-evaporation of material that will not form a silicon eutectic, thus, disrupting nucleation and causing smaller wire formation

[0103] Such methods are utilized in the creation of ultra-high capacity surface based structures through nanofiber growth technology for, e.g., nanofiber based capacitors. Use of single-step metal film type process in creation of nanofibers limits the ability to control the starting metal film thickness, surface roughness, etc., and, thus, the ability of control nucleation from the surface.

[0104] In some embodiments of nanofiber enhanced surfaces it can be desirable to produce multibranched nanofibers. Such multibranched nanofibers could allow an even greater increase in surface area than would occur with non-branched nanofiber surfaces. To produce multibranched nanofibers gold film is optionally deposited onto a nanofiber surface (i.e., one that has already grown nanofibers). When placed in a furnace, fibers perpendicular to the original growth direction can result, thus, generating branches on the original nanofibers. Colloidal metal particles can optionally be used instead of gold film to give greater control of the nucleation and branch formation. The cycle of branching optionally could be repeated multiple times to generate additional branches. Eventually, the branches between adjacent nanofibers could optionally touch and generate an interconnected network. Sintering is optionally used to improve the binding of the fine branches.

[0105] In yet other capacitor embodiments, it is desirable to form finer nanofibers (e.g., nanowires). To accomplish this, some embodiments herein optionally use a non-alloy forming material during gold or other alloy forming metal evaporation. Such material, when introduced in a small percentage can optionally disrupt the metal film to allow it to form smaller droplets during wire growth and, thus, correspondingly finer fibers.

[0106] In yet other embodiments, post processing steps such as vapor deposition of materials can allow for greater anchoring or mechanical adhesion and interconnection between nanofibers, thus, improving mechanical robustness in applications requiring additional strength as well as increasing the overall surface to volume of the nanostructure surface. Additionally, typical embodiments herein have deposition of material(s) to form the dielectric.

[0107] It should be appreciated that specific embodiments and illustrations herein of uses or devices, etc., which comprise nanofiber enhanced surface area capacitors should not be construed as necessarily limiting. In other words, the current invention is illustrated by the descriptions herein, but is not constrained by individual specifics of the descriptions unless specifically stated. The embodiments are illustrative of various uses/applications of the enhanced surface area nanofiber surface capacitors and constructs thereof. Again, the enumeration of specific embodiments herein is not to be taken as necessarily limiting on other uses/applications which comprise the enhanced surface area nanofiber structures of the current invention.

[0108] In some embodiments, the invention comprises methods to selectively modify or create enhanced surface area substrates as well as such enhanced substrates themselves and capacitor devices comprising the same. As will be appreciated, and as is described herein, such methods and devices are applicable to a wide range of uses and can be created in any of a number of ways (several of which are illustrated herein).

[0109] As will be appreciated, the enhanced surface areas provided by surfaces containing nanofibers can provide significant advantages as an integral part of a capacitor. However, in some embodiments, e.g., in manufacturing or as required by some devices, multiple capacitors or multiple nanofiber areas to be incorporated into capacitors are created on the same substrate. Therefore, some embodiments herein comprise methods that can allow spatially controlled chemistry to be applied to nanofiber-enhanced surfaces

(e.g., application of dielectric material(s) and/or material(s) to comprise an opposing electrode plate, etc.), and/or to spatially control the placement of the nanofibers themselves upon the substrate. Such control can facilitate the utility of enhanced nanofiber surfaces in real applications.

[0110] Several approaches are included in the embodiments herein for selectively patterning areas of nanofiber growth or placement on substrates so as to generate spatially defined regions to which to apply specific chemistry (e.g., dielectric deposition). In such approaches, the term "substrate" relates to the material upon which the wires are grown (or, in some embodiments, placed or deposited). In different situations, substrates are optionally comprised of, e.g., silicon wafer, glass, quartz, or any other material appropriate for VLS based nanowire growth or the like. However, in typical embodiments wherein the nanofibers are to be used *in situ*, the substrate is preferably electrically conductive.

[0111] In some embodiments herein, micro-patterning of enhanced surface area substrates is optionally created by lithographically applying planar regions of gold to a substrate as the standard growth initiator through use of conventional lithographic approaches which are well known to those of skill in the art. Nanofibers (e.g., VLS nanowires) are then grown, e.g., in the manner of Peidong Yang, Advanced Materials, Vol. 13, No. 2, Jan. 2001.

[0112] In other embodiments, patterning can be created by chemically precoating a substrate through conventional lithographic approaches so that deposition of gold colloids is controlled prior to growth of nanofibers (e.g., by selective patterning of thiol groups on the substrate surface). In yet other embodiments, nanofibers are optionally pre-grown in a conventional manner well known to those of skill in the art (*see*, e.g., above) and then selectively attached to regions of the substrate where the spatially defined pattern is required. Of course, in yet other embodiments, "lawns" of nanofibers forming an enhanced surface area substrate are selectively patterned through removal of nanofibers in preselected areas. Other embodiments can optionally comprise nanofiber lawns that have areas selectively cleared of nanofibers (thus, creating nanofiber islands, etc.) or can have nanofibers only grown or deposited in certain selected areas (or any combinations thereof). Those of skill in the art will be aware of numerous other patterns, etc. which can optionally be within embodiments herein.

[0113] While, certain methods of patterning, substrate/nanofiber/dielectric/etc. composition and the like are illustrated herein, it will again be appreciated that such are illustrative of the range included in the invention. Thus, such parameters can be changed and still come within the range of the invention. For example, as illustrated above, creation of enhanced surface areas is optionally accomplished in any of a number of ways, all of which are encompassed herein. For example, as described in greater detail in co-pending and commonly assigned U.S. Patent Application Serial No. 60/611,116 entitled "Nanostructured Thin Films and Their Uses," filed September 17, 2004, the entire contents of which are incorporated by reference herein, nanostructured surfaces can be made from a variety of materials including insulating inorganic materials such as a native oxide layer or a deposited oxide or nitride layer. The insulating inorganic material may also be formed form a deposited metal layer. For example, the insulating inorganic material may be selected from the group of materials including aluminum (Al), alumina (Al_2O_3), ZnO, SiO_2, ZrO_2, HfO_2, a hydrous form of these oxides, a compound oxide such as $SiTiO_3$, $BaTiO_3$ $PbZrO_4$ or a silicate. In one example, the film layer is made from alumina or aluminum which can be deposited on the substrate (e.g., one or more electrode plates) using a variety of well-known techniques such as thermal evaporation and sputtering including physical vapor deposition (PVD), sputter deposition, chemical vapor deposition (CVD), metallorganic CVD, plasma-enhanced CVD, laser ablation, or solution deposition methods such as spray coating, dip coating, or spin coating etc. Ultra-thin metal films (e.g., films less than about 5nm in thickness) may be deposited by atomic layer deposition (ALD) techniques. The thin film preferably has a thickness less than about 1000 nm, for example, between about 5 and 400 nm, for example, between about 5 and 200 nm, for example, between about 10 and 100 nm. The film layer may then be configured to have a nanostructured surface, for example, by boiling the film layer, autoclaving it, etc. for a sufficient time (e.g., between about 3 to 60 minutes, for example, between about 5 to 30 minutes) to convert the film into a highly ordered nanostructured surface having pore sizes less than about 200 nm. The nanostructured film layer can also be formed by other means such as the formation of porous alumina films via the anodization of aluminum metal in acidic solution (e.g., phosphoric, oxalic, or sulfuric acid solutions). *See*, e.g., Evelina Palibroda, A. Lupsan, Stela Pruneanu, M. Savos, *Thin Solid Films* , 256, 101 (1995), the entire contents of which are incorporated by reference herein. Other textured surfaces other than alumina or aluminum can also be used including, for

example, zinc oxide (ZnO) nanostructured surfaces and the other material surfaces described above. Low-temperature solution-based approaches to forming ZnO nanotextured surfaces are described, for example, in "Low Temperature Wafer-Scale Production of ZnO Nanowire Arrays," Lori E. Greene et al., Angew. Chem. Int. Ed. 2003, 42, 3031-3034, the entire contents of which are incorporated by reference herein.

[0114] The nanostructured film layer can also optionally be coated or functionalized, e.g., to enhance or add specific properties. For example, polymers, ceramics, or small molecules can optionally be used as coating materials. The optional coatings can impart characteristics such as water resistance, improved mechanical, optical (e.g., enhancement of light coupling) or electrical properties. The nanostructured film layer may also be derivatized with one or more functional moieties (e.g., a chemically reactive group) such as one or more silane groups, e.g., one or more per-fluorinated silane groups, or other coatings such as diamond coatings, a hydrocarbon molecule, a fluorocarbon molecule, or a short chain polymer of both types of molecules which may be attached to the film layer via silane chemistry. Those of skill in the art will be familiar with numerous functionalizations and functionalization techniques which are optionally used herein (e.g., similar to those used in construction of separation columns, bio-assays, etc.).

[0115] For example, details regarding relevant moiety and other chemistries, as well as methods for construction/use of such, can be found, e.g., in Hermanson Bioconjugate Techniques Academic Press (1996), Kirk-Othmer Concise Encyclopedia of Chemical Technology (1999) Fourth Edition by Grayson et al. (ed.) John Wiley & Sons, Inc., New York and in Kirk-Othmer Encyclopedia of Chemical Technology Fourth Edition (1998 and 2000) by Grayson et al. (ed.) Wiley Interscience (print edition)/ John Wiley & Sons, Inc. (e-format). Further relevant information can be found in CRC Handbook of Chemistry and Physics (2003) 83rd edition by CRC Press. Details on conductive and other coatings, which can also be incorporated onto the nanostructured film layer of the invention by plasma methods and the like can be found in H. S. Nalwa (ed.), Handbook of Organic Conductive Molecules and Polymers, John Wiley & Sons 1997. *See* also, "ORGANIC SPECIES THAT FACILITATE CHARGE TRANSFER TO/FROM NANOCRYSTALS," USSN 60/452,232 filed March 4, 2003 by Whiteford et al. Details regarding organic chemistry, relevant for, e.g., coupling of additional moieties to a

functionalized surface can be found, e.g., in Greene (1981) Protective Groups in Organic Synthesis, John Wiley and Sons, New York, as well as in Schmidt (1996) Organic Chemistry Mosby, St Louis, MO, and March's Advanced Organic Chemistry Reactions, Mechanisms and Structure, Fifth Edition (2000) Smith and March, Wiley Interscience New York ISBN 0-471-58589-0, and Attorney Docket No. 40-002410US filed April 27, 2004, entitled "Super-hydrophobic Surfaces, Methods of Their Construction and Uses Therefor." Those of skill in the art will be familiar with many other related references and techniques amenable for functionalization of surfaces herein.

[0116] While the foregoing invention has been described in some detail for purposes of clarity and understanding, it will be clear to one skilled in the art from a reading of this disclosure that various changes in form and detail can be made without departing from the true scope of the invention. For example, all the techniques and apparatus described above can be used in various combinations. All publications, patents, patent applications, or other documents cited in this application are incorporated by reference in their entirety for all purposes to the same extent as if each individual publication, patent, patent application, or other document were individually indicated to be incorporated by reference for all purposes.

CLAIMS

What is claimed is:

1. An electric capacitor, comprising at least a first electrode surface, which electrode surface comprises a plurality of nanofibers.

2. The capacitor of claim 1, wherein the surface comprises a conductive material.

3. The capacitor of claim 2, wherein the conductive material comprises a metal, a semiconducting material, a polymer, or a resin.

4. The capacitor of claim 1, wherein one or more of the surface or the members of the plurality of nanofibers comprises silicon.

5. The capacitor of claim 1, wherein the plurality of nanofibers comprises the same composition as the composition of the first surface.

6. The capacitor of claim 1, wherein the plurality of nanofibers comprises a different composition from the composition of the first surface.

7. The capacitor of claim 1, wherein the plurality of nanofibers is grown on the face of the surface.

8. The capacitor of claim 1, wherein the plurality of nanofibers is deposited on the face of the surface.

9. The capacitor of claim 1, further comprising a dielectric which comprises a nonconductive material and which covers substantially all members of the plurality of nanofibers.

10. The capacitor of claim 9, wherein the dielectric comprises an oxide, a nitride, a polymer, a ceramic, a resin, a porcelain, a mica containing material, a glass, a vacuum, a rare earth oxide, a gas, or other typical dielectrics used in electronic capacitors.

11. The capacitor of claim 10, wherein the dielectric comprises a grown oxide layer.

12. The capacitor of claim 10, wherein the dielectric comprises a naturally occurring oxide layer.

13. The capacitor of claim 10, wherein the dielectric comprises silicon oxide.

14. The capacitor of claim 10, wherein the oxide layer comprises a thickness of from about 1 nm or less to about 1 um, from about 2 nm or less to about 750 nm, from about 5 nm or less to about 500 nm, from about 10 nm or less to about 250 nm, or from about 50 nm or less to about 100 um.

15. The capacitor of claim 10, wherein the oxide layer comprises a thickness substantially equivalent to the thickness of the electrode surface.

16. The capacitor of claim 1, further comprising a second electrode surface, which second surface comprises a layer of material deposed upon the dielectric covering the plurality of nanofibers.

17. The capacitor of claim 16, wherein the second surface material comprises a conductive material.

18. The capacitor of claim 17, wherein the second surface comprises a metal, a semiconducting material, a polymer, or a resin.

19. The capacitor of claim 18, wherein the second surface comprises an evaporated or sputtered electrically conducting material.

20. The capacitor of claim 19, wherein the electrically conducting material comprises aluminum, tantalum, platinum, nickel, a semiconducting material, polysilicon, titanium, titanium oxide, an electrolyte, or gold.

21. The capacitor of claim 1, wherein a density of the members of the plurality of nanofibers ranges from about 0.11 nanofiber per square micron or less to at least about 1000 nanofibers per square micron, from about 1 nanofiber per square micron

or less to at least about 500 nanofibers per square micron, from about 10 nanofibers per square micron or less to at least about 250 nanofibers per square micron, or from about 50 nanofibers per square micron or less to at least about 100 nanofibers per square micron.

22. The capacitor of claim 1, wherein a length of the members of the plurality of nanofibers ranges from about 1 micron or less to at least about 500 microns, from about 5 micron or less to at least about 150 microns, from about 10 micron or less to at least about 125 microns, or from about 50 micron or less to at least about 100 microns; and wherein the diameter of the members of the plurality of nanofibers ranges from about 5 nm or less to at least about 1 micron, from about 10 nm or less to at least about 500 nm, from about 20 nm or less to at least about 250 nm, from about 20 nm or less to at least about 200 nm, from about 40 nm or less to at least about 200 nm, from about 50 nm or less to at least about 150 nm, or from about 75 nm or less to at least about 100 nm.

23. The capacitor of claim 1, wherein a density of the members of the plurality of nanofibers increases the surface area of the first electrode surface at least 1.5 times to at least 100,00 times or more, at least 5 times to at least 75, 000 times or more, at least 10 times to at least 50,000 times or more, at least 50 times to at least 25,000 times or more, at least 100 times to at least 10,000 times or more, or at least 500 times to at least 1,000 times or more greater in comparison to an area of electrode surface without nanofibers, which area comprises a substantially equal footprint.

24. The capacitor of claim 1, wherein the farad capacity of the capacitor comprises from about at least 1.5 times to at least 100,00 times or more, at least 5 times to at least 75, 000 times or more, at least 10 times to at least 50,000 times or more, at least 50 times to at least 25,000 times or more, at least 100 times to at least 10,000 times or more, or at least 500 times to at least 1,000 times or more greater in capacity in relation to a capacitor having an electrode surface of substantially equal footprint but not comprising a plurality of nanofibers.

25. A device comprising the capacitor of claim 1, 9, or 16.

26. The device of claim 25, wherein the device comprises a timepiece, a watch, a radio, a remote control device, a nanodevice, a medical prosthetic, or a medical implant device.

27. A capacitor comprising a supporting substrate having at least a first electrode surface, a nanostructured thin film layer deposited on at least a region of the surface, and a hydrophobic coating deposited on the film layer.

28. The capacitor of claim 27, wherein the film layer comprises alumina or aluminum.

29. The capacitor of claim 27, wherein the hydrophobic coating comprises a diamond-like carbon coating.

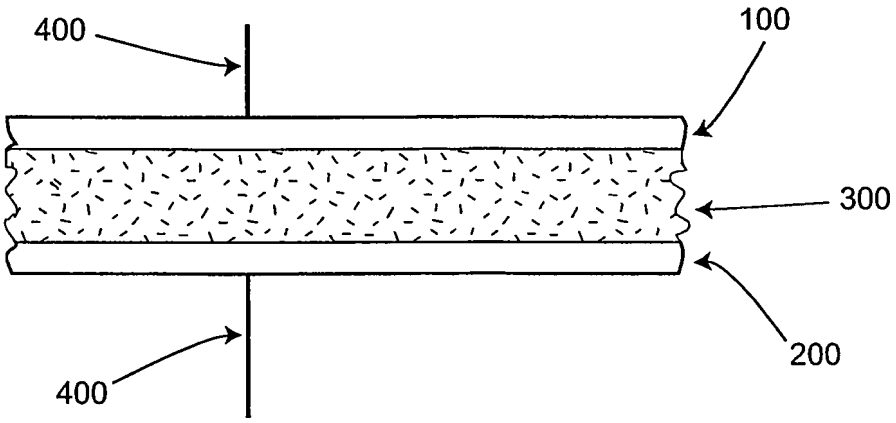

Fig. 1

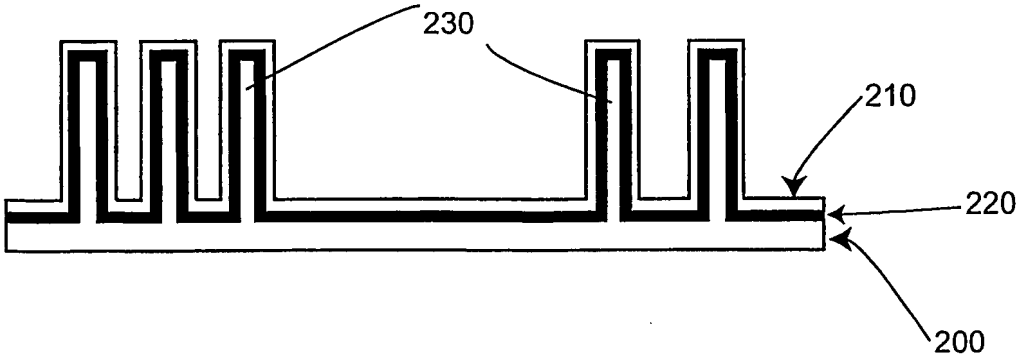

Fig. 2

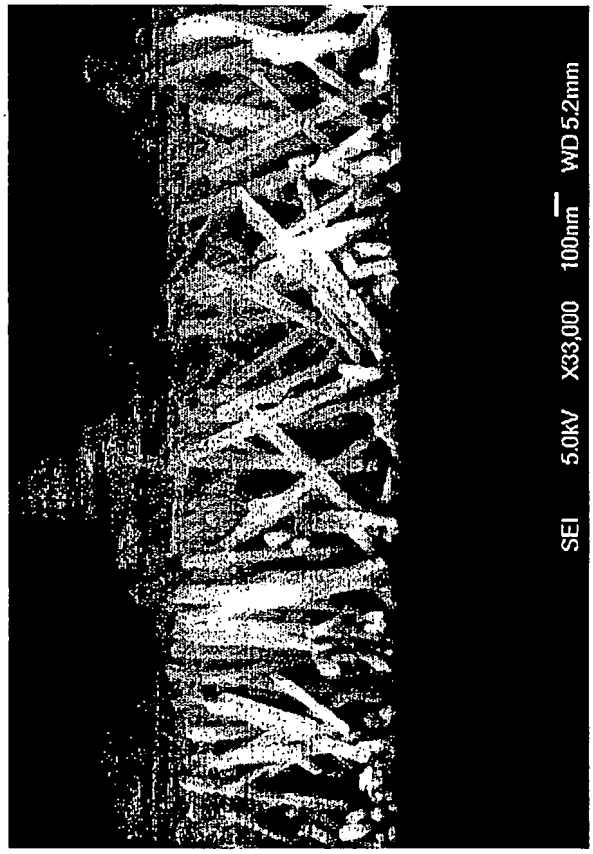

Fig. 3B

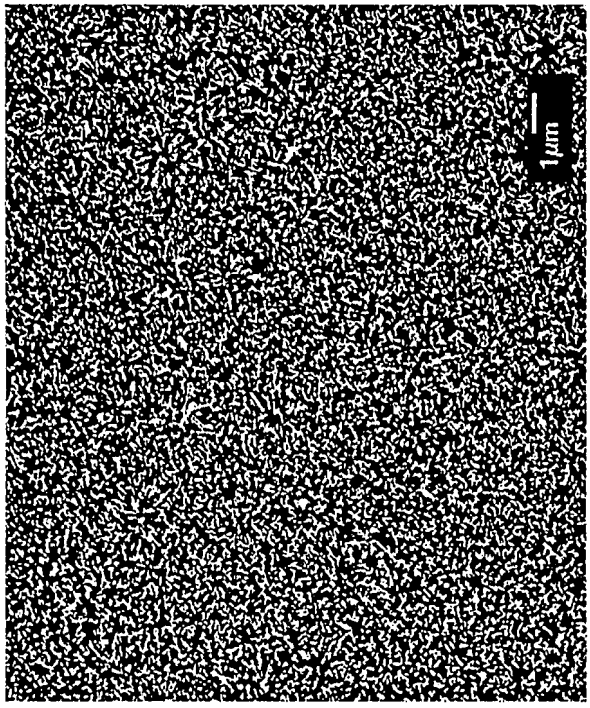

Fig. 3A

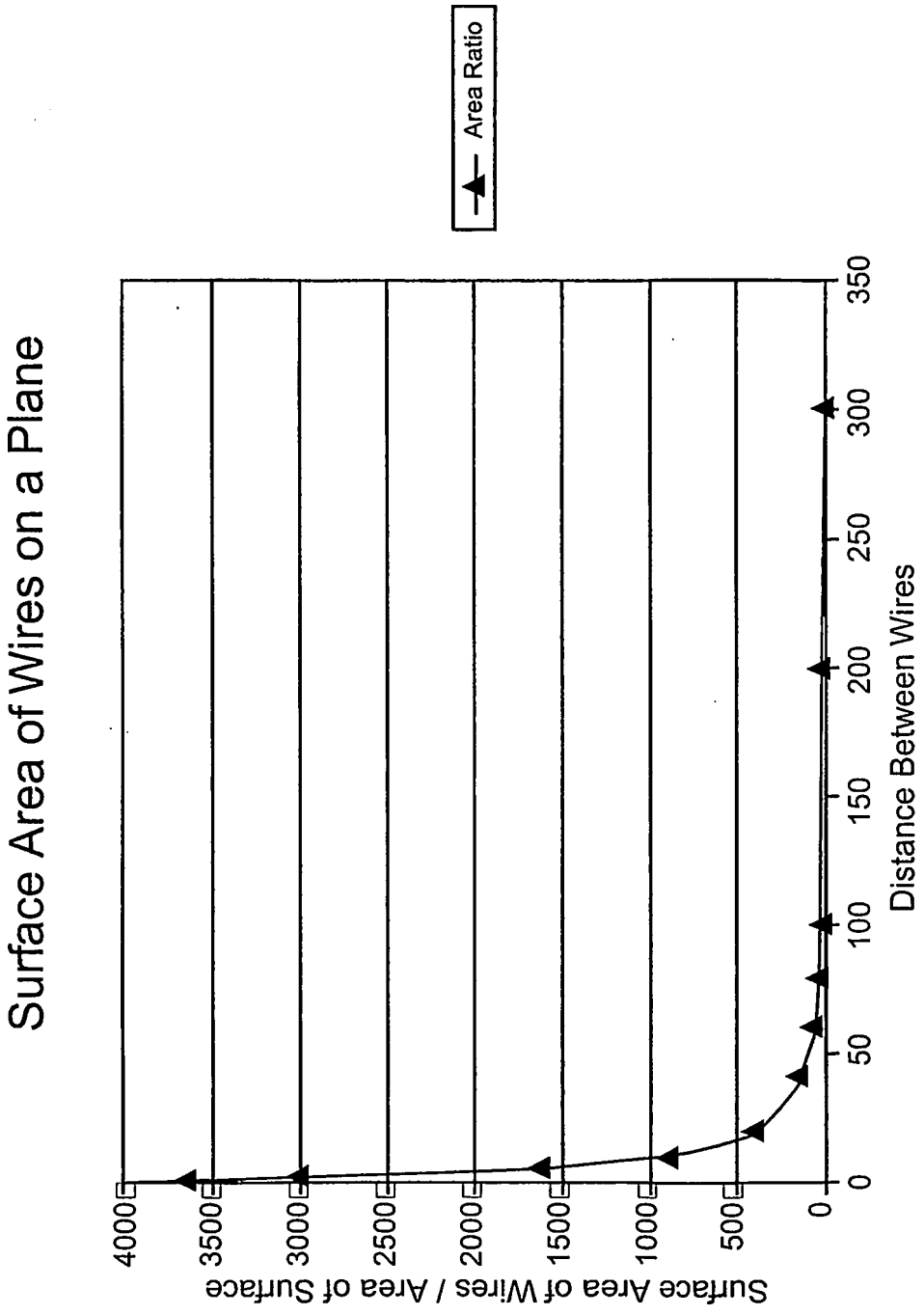
Surface Area of Wires on a Plane
Area Ratio
Surface Area of Wires / Area of Surface
4000
3500
3000
2500
2000
1500
1000
500
0
0
50
100
150
200
250
300
350
Distance Between Wires

Fig. 4

NANOSTRUCTURES CONTAINING METAL-SEMICONDUCTOR COMPOUNDS

FEDERALLY SPONSORED RESEARCH

The present invention was sponsored by DARPA, Grant No. N-00014-01-1-0651. The U.S. Government may have certain rights to the present invention.

FIELD OF INVENTION

The present invention relates generally to nanotechnology and sub-microelectronic circuitry, as well as associated methods and devices. In particular, the present invention relates to components for use in nanotechnology and sub-microelectronic circuitry that include metal-semiconductor compounds such as metal silicides. Articles and devices of size greater than the nanoscale are also included.

DISCUSSION OF RELATED ART

Interest in nanotechnology, in particular sub-microelectronic technologies such as semiconductor quantum dots and nanowires, has been motivated by the challenges of chemistry and physics at the nanoscale, and by the prospect of utilizing these structures in electronic, optical, and other related devices. Nanoscopic articles may be well-suited for transport of charge carriers and excitons (e.g. electrons, electron hole pairs, etc.) and thus may be useful as building blocks in nanoscale electronics, optics, and other applications.

SUMMARY OF INVENTION

The present invention generally relates to components for use in nanotechnology and sub-microelectronic circuitry that include metal-semiconductor compounds such as metal silicides. Most aspects and embodiments of the present invention involve nanometer-scale articles and devices, but larger articles and devices are provided as well. The subject matter of the present invention involves, in some cases, interrelated products, one or more solutions to a particular problem, and/or a plurality of different uses of one or more systems and/or articles.

In one aspect, the present invention is a method. In one set of embodiments, the method includes providing a bulk metal adjacent a semiconductor wire, and diffusing at least a portion of the bulk metal into at least a portion of the semiconductor wire and thereby changing that portion from a semiconductor to a conductor, where the

semiconductor wire comprises at least one portion having a smallest dimension of less than about 500 nm. The method, in another set of embodiments, includes diffusing a material into at least a portion of a wire, where the wire comprises at least one portion having a smallest dimension of less than about 500 nm.

The method, according to another set of embodiments, includes an act of diffusing a metal into at least a portion of a semiconductor nanoscale wire to form a stoichiometric ratio of metal atoms to semiconductor atoms within the portion of the semiconductor nanoscale wire. In yet another set of embodiments, the method includes an act of bulk-doping at least a portion of a nanoscale wire after growth of the nanoscale wire. The method, in still another set of embodiments, includes an act of diffusing a material into a center portion of a semiconductor wire. In some cases, the semiconductor wire comprises at least one portion having a smallest dimension of less than about 500 nm. In one embodiment, the method includes an act of converting a conductor into a semiconductor. In another embodiment, the method includes an act of converting a semiconductor into a conductor.

The present invention includes an article in another aspect. In one set of embodiments, the article includes a wire or other nanostructure. In one embodiment, the wire or nanostructure comprises at least one metal silicide, where the wire or other nanostructure is a single crystal. In another embodiment, the wire or other nanostructure includes a compound having a stoichiometric ratio of silicon and at least one metal. In some cases, the wire or other nanostructure has at least one portion having a smallest dimension of less than about 500 nm. The wire or other nanostructure, in another embodiment, comprises at least one metal silicide having a resistivity of less than about 60 microOhm cm. In some cases, the wire or other nanostructure may have resistivity of less than about 60 microOhm cm. In yet another embodiment, the wire or other nanostructure includes at least one metal silicide able to carry a current density of at least about 10^8 A/cm^2. In certain instances, the wire or other nanostructure is able to carry a current density of at least about 10^8 A/cm^2.

In another embodiment, the wire or other nanostructure comprises at least two regions differing in composition, where at least one region comprising a metal silicide, and where the wire or other nanostructure comprises at least one portion having a smallest dimension of less than about 500 nm. In still another embodiment, the wire or other nanostructure includes at least two regions that differ in composition and a

boundary between the regions, where the boundary has a maximum dimension of less than about 500 nm and at least one region comprises a metal silicide.

In another aspect, the present invention is directed to a method of making one or more of the embodiments described herein, for example, a nanoscale wire comprising a metal silicide. In yet another aspect, the present invention is directed to a method of using one or more of the embodiments described herein. In still another aspect, the present invention is directed to a method of promoting one or more of the embodiments described herein.

Other advantages and novel features of the present invention will become apparent from the following detailed description of various non-limiting embodiments of the invention when considered in conjunction with the accompanying figures. In cases where the present specification and a document incorporated by reference include conflicting and/or inconsistent disclosure, the present specification shall control.

BRIEF DESCRIPTION OF DRAWINGS

Non-limiting embodiments of the present invention will be described by way of example with reference to the accompanying figures, which are schematic and are not intended to be drawn to scale. In the figures, each identical or nearly identical component illustrated is typically represented by a single numeral. For the purposes of clarity, not every component is labeled in every figure, nor is every component of each embodiment of the invention shown where illustration is not necessary to allow those of ordinary skill in the art to understand the invention. In the figures:

Fig. 1A is a schematic diagram of a technique used to prepare a nanowire comprising a metal-semiconductor compound, in accordance with one embodiment of the invention;

Figs. 1B-1D are photomicrographs of various nanowires comprising metal-semiconductor compounds;

Figs. 2A-2B illustrate graphs of current versus voltage for certain nanowires of the invention

Fig. 3A is a schematic diagram of a method of making a nanowire that includes at least one heterojunction, according to an embodiment of the invention;

Figs. 3B-3D are photomicrographs of certain nanowires of the invention having heterojunctions, where each nanowire includes at least one region that comprises a metal-semiconductor compound;

Fig. 4A is a graph of current versus voltage for a nanowire including a heterojunction, where at least one region of the nanowire comprises a metal-semiconductor compound, in accordance with one embodiment of the invention;

Figs. 4B-4D illustrate various nanowires that include heterojunctions, useful as transistors;

Figs. 5A-5C are schematic diagrams illustrating one embodiment of the invention;

Figs. 6A-6F illustrate other methods of making a nanowire that includes at least one heterojunction, according to another embodiment of the invention; and

Figs. 7A-7G illustrate certain silicide nanowires of the invention, and their performance characteristics.

DETAILED DESCRIPTION

The present invention generally relates to devices and components for use in nanotechnology and sub-microelectronic circuitry that include metal-semiconductor compounds such as metal silicides. The present invention also, in some embodiments, provides methods of forming such devices and components by allowing a first material to diffuse into a second material, optionally creating a new compound. Thus, as an example, metal atoms are allowed to diffuse into a semiconductor to create the metal-semiconductor compound. In some cases, the device may include a component that is a single crystal. Certain metal-semiconductor compounds of the invention have novel physical/electrical properties, for example, low resistivities, high conductivities, high current density capacities, and the like. In some embodiments, a component of the invention may have two or more regions that differ in composition, where one or both of the regions can include a metal-semiconductor compound. In some cases, the regions may be created by using a mask or a nanoscale wire to define the two or more regions.

The indefinite articles "a" and "an," as used herein in the specification and in the claims, unless clearly indicated to the contrary, should be understood to mean "at least one." As used herein, "or" should be understood to mean inclusively or, i.e., the inclusion of at least one, but including more than one, of a number or list of elements. Only terms clearly indicated to the contrary, such as "only one of" or "exactly one of," will refer to the inclusion of exactly one element of a number or list of elements. The term "plurality," as used herein, means two or more. A "set" of items may include one or more of such items.

The term "fluid" generally refers to a substance that tends to flow and to conform to the outline of its container. Typically, fluids are materials that are unable to withstand a static shear stress. When a shear stress is applied to a fluid, it experiences a continuing and permanent distortion. Typical fluids include liquids and gasses, but may also include free-flowing solid particles, viscoelastic fluids, and the like.

Certain devices of the invention may include wires or other components of scale commensurate with nanometer-scale wires, which includes nanotubes and nanowires. In some embodiments, however, the invention comprises articles that may be greater than nanometer size (e. g., micrometer-sized). As used herein, "nanoscopic-scale," "nanoscopic," "nanometer-scale," "nanoscale," the "nano-" prefix (for example, as in "nanostructured"), and the like generally refers to elements or articles having widths or diameters of less than about 1 micron, and less than about 100 nm in some cases. In all embodiments, specified widths can be a smallest width (i.e. a width as specified where, at that location, the article can have a larger width in a different dimension), or a largest width (i.e. where, at that location, the article has a width that is no wider than as specified, but can have a length that is greater).

As used herein, a "wire" generally refers to any material having a conductivity of any semiconductor or any metal, and in some embodiments may be used to connect two electronic components such that they are in electronic communication with each other. For example, the term "electrically conductive" or a "conductor" or an "electrical conductor" when used with reference to a "conducting" wire or a nanoscale wire, refers to the ability of that wire to pass charge. In certain instances, the electrically conductive material can have a resistivity lower than about 10^5 microOhm cm ($\mu\Omega$ cm), lower than about 10^4 microOhm cm, lower than about 10^3 microOhm cm, lower than about 100 microOhm cm, or lower than about 10 microOhm cm.

A "nanoscopic wire" (also known herein as a "nanoscopic-scale wire" or "nanoscale wire") generally is a wire, that at any point along its length, has at least one cross-sectional dimension and, in some embodiments, two orthogonal cross-sectional dimensions less than 1 micron, less than about 500 nm, less than about 200 nm, less than about 150 nm, less than about 100 nm, less than about 70, less than about 50 nm, less than about 20 nm, less than about 10 nm, or less than about 5 nm. In other embodiments, the cross-sectional dimension can be less than 2 nm or 1 nm. In one set of embodiments, the nanoscale wire has at least one cross-sectional dimension ranging from 0.5 nm to 200

nm. Where nanoscale wires are described having, for example, a core and an outer region, the above dimensions generally relate to those of the core. The cross-section of a nanoscopic wire may be of any arbitrary shape, including, but not limited to, circular, square, rectangular, annular, polygonal, or elliptical, and may be a regular or an irregular shape. The nanoscale wire may be solid or hollow. Any nanoscale wire can be used in any of the embodiments described herein, including carbon nanotubes, nanorods, nanowires, nanowhiskers, organic or inorganic conductive or semiconducting polymers, and the like, unless otherwise specified. Other conductive or semiconducting elements that may not be molecular wires, but are of various small nanoscopic-scale dimensions, can also be used in some instances, e.g. inorganic structures such as main group and metal atom-based wire-like silicon, transition metal-containing wires, gallium arsenide, gallium nitride, indium phosphide, germanium, cadmium selenide, etc. A wide variety of these and other nanoscale wires can be grown on and/or applied to surfaces in patterns useful for electronic devices in a manner similar to techniques described herein involving nanoscale wires, without undue experimentation. The nanoscale wires, in some cases, may be formed having dimensions of at least about 1 micron, at least about 3 microns, at least about 5 microns, or at least about 10 microns or about 20 microns in length, and can be less than about 100 nm, less than about 75 nm, less than about 50 nm, or less than about 25 nm in thickness (height and width). The nanoscale wires may have an aspect ratio (length to thickness) of greater than about 2:1, greater than about 3:1, greater than about 5:1, greater than about 10:1, greater than about 25:1, greater than about 50:1, greater than about 75:1, greater than about 100:1, greater than about 150:1, greater than about 250:1, greater than about 500:1, greater than about 750:1, or greater than about 1000:1 or more in some cases.

A "nanowire" (e. g. comprising silicon and/or another semiconductor material, for example, a metal-semiconductor compound such as NiSi) is a nanoscopic wire that is generally a solid wire, and may be elongated in some cases. Preferably, a nanowire (which is abbreviated herein as "NW") is an elongated semiconductor, i.e., a nanoscale semiconductor. A "non-nanotube nanowire" is any nanowire that is not a nanotube. In one set of embodiments of the invention, a non-nanotube nanowire having an unmodified surface is used in any arrangement of the invention described herein in which a nanowire or nanotube can be used.

As used herein, a "nanotube" (e.g. a carbon nanotube) is generally nanoscopic wire that is hollow, or that has a hollowed-out core, including those nanotubes known to those of ordinary skill in the art. "Nanotube" is abbreviated herein as "NT." Nanotubes are used as one example of small wires for use in the invention and, in certain embodiments, devices of the invention include wires of scale commensurate with nanotubes.

As used herein, an "elongated" article (e.g. a semiconductor or a section thereof) is an article for which, at any point along the longitudinal axis of the article, the ratio of the length of the article to the largest width at that point is greater than 2:1.

As used herein, a "width" of an article is the distance of a straight line from a point on a perimeter of the article, through the center of the article, to another point on the perimeter of the article. As used herein, a "width" or a "cross-sectional dimension" at a point along a longitudinal axis of an article is the distance along a straight line that passes through the center of a cross-section of the article at that point and connects two points on the perimeter of the cross-section. The "cross-section" at a point along the longitudinal axis of an article is a plane at that point that crosses the article and is orthogonal to the longitudinal axis of the article. The "longitudinal axis" of an article is the axis along the largest dimension of the article. Similarly, a "longitudinal section" of an article is a portion of the article along the longitudinal axis of the article that can have any length greater than zero and less than or equal to the length of the article. Additionally, the "length" of an elongated article is a distance along the longitudinal axis from end to end of the article.

As used herein, a "cylindrical" article is an article having an exterior shaped like a cylinder, but does not define or reflect any properties regarding the interior of the article. In other words, a cylindrical article may have a solid interior, may have a hollowed-out interior, etc. Generally, a cross-section of a cylindrical article appears to be circular or approximately circular, but other cross-sectional shapes are also possible, such as a hexagonal shape. The cross-section may have any arbitrary shape, including, but not limited to, square, rectangular, or elliptical. Regular and irregular shapes are also included.

As used herein, an "array" of articles (e.g., nanoscopic wires) comprises a plurality of the articles, for example, a series of aligned nanoscale wires, which may or may not be in contact with each other. As used herein, a "crossed array" or a "crossbar

array" is an array where at least one of the articles contacts either another of the articles or a signal node (e.g., an electrode).

Many nanoscopic wires as used in accordance with the present invention are individual nanoscopic wires. As used herein, "individual nanoscopic wire" means a nanoscopic wire free of contact with another nanoscopic wire (but not excluding contact of a type that may be desired between individual nanoscopic wires, e.g., as in a crossbar array). For example, an "individual" or a "free-standing" article may, at some point in its life, not be attached to another article, for example, with another nanoscopic wire, or the free-standing article may be in solution. This is in contrast to nanotubes produced primarily by laser vaporization techniques that produce materials formed as ropes having diameters of about 2 nm to about 50 nm or more and containing many individual nanotubes (see, for example, Thess, *et al.*, "Crystalline Ropes of Metallic Carbon Nanotubes," *Science*, 273:483-486 (1996), incorporated herein by reference in its entirety for all purposes). This is also in contrast to conductive portions of articles which differ from surrounding material only by having been altered chemically or physically, *in situ*, i.e., where a portion of a uniform article is made different from its surroundings by selective doping, etching, etc. An "individual" or a "free-standing" article is one that can be (but need not be) removed from the location where it is made, as an individual article, and transported to a different location and combined with different components to make a functional device such as those described herein and those that would be contemplated by those of ordinary skill in the art upon reading this disclosure.

In some embodiments, at least a portion of a nanoscopic wire may be a bulk-doped semiconductor. As used herein, a "bulk-doped" article (e. g. an article, or a section or region of an article) is an article for which a dopant is incorporated substantially throughout the crystalline lattice of the article, as opposed to an article in which a dopant is only incorporated in particular regions of the crystal lattice at the atomic scale, for example, only on the surface or exterior. For example, some articles such as carbon nanotubes are typically doped after the base material is grown, and thus the dopant only extends a finite distance from the surface or exterior into the interior of the crystalline lattice. It should be understood that "bulk-doped" does not define or reflect a concentration or amount of doping in a semiconductor, nor does it necessarily indicate that the doping is uniform. In particular, in some embodiments, a bulk-doped semiconductor may comprise two or more bulk-doped regions. Thus, as used herein to

describe nanoscopic wires, "doped" refers to bulk-doped nanoscopic wires, and, accordingly, a "doped nanoscopic (or nanoscale) wire" is a bulk-doped nanoscopic wire. "Heavily doped" and "lightly doped" are terms the meanings of which are clearly understood by those of ordinary skill in the art.

The present invention, in one aspect, includes a nanoscopic wire or other nanostructured material comprising a metal-semiconductor compound. The nanoscopic wire may be, for example, a nanorod, a nanowire, a nanowhisker, or a nanotube. The nanoscopic wire may be used in a device, for example, as a semiconductor component, a pathway, etc. In some cases, the nanoscopic wire may further include, in addition to the metal-semiconductor compound, materials such as semiconductors, dopants, etc.

As used herein, a "metal-semiconductor compound" is a compound that includes at least one metal combined with a semiconductor. In metal-semiconductor compounds of the invention, at least one portion of the compound includes a metal and a semiconductor present in a stoichiometrically defined ratio, i.e., the metal atoms and the semiconductor atoms are present within the compound (i.e., on the atomic scale) in a whole number ratio that is chemically defined, i.e., defined on the basis of the atomic interactions between the metal atoms and the semiconductor atoms within the compound that lead to a ratio of elements present dictated by the bonding principles of chemistry (e.g. coordination chemistry, atomic and molecular orbital interactions and formation, crystal packing, and/or the like). This is to be distinguished from alloys or mixtures, which are simply blends of two or more atoms in a substance, in which the atoms can be mixed together in any ratio, where the ratio is not determined by stoichiometric interactions between the atoms, and doping, where, e.g., ion bombardment of a material with a dopant leads to non-stoichiometric amounts of the dopant in the host material dictated by the amount of dopant introduced. Instead, the metal atoms and the semiconductor atoms in a metal-semiconductor compound interact on the atomic level in a defined fashion, thus resulting in the metal-semiconductor compound having a whole number ratio between the metal atoms and the semiconductor atoms within the compound, i.e., the ratio is dictated by atomic interactions between the metal atoms and the semiconductor atoms within the compound. Thus, the stoichiometric ratio between the metal atoms and the semiconductor atoms is always the same on the atomic level (i.e., at any location within the compound). As an example, there may be ionic charged interactions between the metal atoms and the semiconductor atoms such that, for charge

neutrality, there is a stoichiometric ratio between the metal atoms and the semiconductor atoms within the compound, for example, MZ, M_2Z, M_2Z_3, MZ_2, M_3Z_2, or the like, where M is a metal and Z is a semiconductor. A specific non-limiting example is nickel silicide, NiSi. In some cases, more than one type of metal atom and/or more than one type of semiconductor atom may be present in the metal-semiconductor compound. It should be recognized, of course, that measurements of the ratio of two or more atoms in a compound are not necessarily always exact, due to experimental error and other practical limitations. Thus, in some cases, the ratio so measured may be stoichiometric in reality, even though the experimental measurements deviate somewhat from whole number ratios. As an example, the actual ratios determined for a metal-semiconductor compound may be within about 10% or about 5% of a stoichiometric, whole number ratio.

In one set of embodiments, the metal within the metal-semiconductor compound is a transition metal, for example, an element from one or more of Group IB, Group IIB, Group IIIB, Group IVB, Group VB, Group VIB, Group VIIB, or Group VIIIB. In some cases, Group VIIIB metals may be particularly useful within the metal-semiconductor compound, for example, nickel, iron, palladium, platinum, iridium, etc.

As used herein, the term "Group," with reference to the Periodic Table, is given its usual definition as understood by one of ordinary skill in the art. For instance, the Group II elements include Mg and Ca, as well as the Group II transition elements, such as Zn, Cd, and Hg. Similarly, the Group III elements include B, Al, Ga, In and Tl; the Group IV elements include C, Si, Ge, Sn, and Pb; the Group V elements include N, P, As, Sb and Bi; and the Group VI elements include O, S, Se, Te and Po. Combinations involving more than one element from each Group are also possible. For example, a Group II-VI material may include at least one element from Group II and at least one element from Group VI, for example, ZnS, ZnSe, ZnSSe, ZnCdS, CdS, or CdSe. Similarly, a Group III-V material may include at least one element from Group III and at least one element from Group V, for example GaAs, GaP, GaAsP, InAs, InP, AlGaAs, or InAsP. Other dopants may also be included with these materials and combinations thereof, for example, transition metals such as Fe, Co, Te, Au, and the like. As used herein, transition metal groups of the periodic table, when referred to in isolation (i.e., without referring to the main group elements), are indicated with a "B." The transition metals elements include the Group IB elements (Cu, Ag, Au), the Group IIB elements

(Zn, Cd, Hg), the Group IIIB elements (Sc, Y, lanthanides, actinides), the Group IVB elements (Ti, Zr, Hf), the Group VB elements (V, Nb, Ta), the Group VIB elements (Cr, Mo, W), the Group VIIB elements (Mn, Tc, Re), and the Group VIIIB elements (Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt).

As used herein, a "semiconductor" is given its ordinary meaning in the art, i.e., an element having semiconductive or semi-metallic properties (i.e., between metallic and non-metallic properties). An example of a semiconductor is silicon. Other non-limiting examples include gallium, germanium, diamond (carbon), tin, selenium, tellurium, boron, or phosphorous.

In one set of embodiments, the invention includes a nanoscale wire (or other nanostructured material) that is a single crystal. As used herein, a "single crystal" item (e.g., a semiconductor) is an item that has covalent bonding, ionic bonding, or a combination thereof throughout the item. Such a single-crystal item may include defects in the crystal, but is to be distinguished from an item that includes one or more crystals, not ionically or covalently bonded, but merely in close proximity to one another. Techniques for producing such nanoscale wires are further discussed below.

The nanoscale wire may also have certain novel physical properties in some embodiments. The enhanced physical properties of the nanoscale wires of the invention may be due to the crystallinity of the nanowires (for example, a nanoscale wire having very few crystal domains, and in some cases, the nanoscale wire being a single crystal), quantum effects (e.g., due to the size of the nanoscale wire), or the like. For instance, in some cases, a nanoscale wire of the invention may have very low resistivities, for example, resistivities of less than about 100 microOhm cm ($\mu\Omega$ cm) and in some cases, less than about 80 microOhm cm, less than about 60 microOhm cm, less than about 40 microOhm cm, less than about 20 microOhm cm or less than about 10 microOhm cm. In another set of embodiments, the nanowire of the invention may be able to carry very high current densities without breakage or mechanical failure. For example, a nanowire of the invention may be able to carry current densities of at least about $10^7 A/cm^2$, and in some cases, greater than about $10^8 A/cm^2$, or greater than about $10^9 A/cm^2$ without breakage or mechanical failure.

In another set of embodiments, the nanoscopic wire (or other nanostructured material) comprising a metal-semiconductor compound may include additional materials, such as semiconductor materials, dopants, organic compounds, inorganic compounds,

etc. The following are non-limiting examples of materials that may be used as dopants within the nanoscopic wire. The dopant may be an elemental semiconductor, for example, silicon, germanium, tin, selenium, tellurium, boron, diamond, or phosphorous. The dopant may also be a solid solution of various elemental semiconductors. Examples include a mixture of boron and carbon, a mixture of boron and $P(BP_6)$, a mixture of boron and silicon, a mixture of silicon and carbon, a mixture of silicon and germanium, a mixture of silicon and tin, a mixture of germanium and tin, etc. In some embodiments, the dopant may include mixtures of Group IV elements, for example, a mixture of silicon and carbon, or a mixture of silicon and germanium. In other embodiments, the dopant may include mixtures of Group III and Group V elements, for example, BN, BP, BAs, AlN, AlP, AlAs, AlSb, GaN, GaP, GaAs, GaSb, InN, InP, InAs, or InSb. Mixtures of these combinations may also be used, for example, a mixture of BN/BP/BAs, or BN/AlP. In other embodiments, the dopants may include mixtures of Group III and Group V elements. For example, the mixtures may include AlGaN, GaPAs, InPAs, GaInN, AlGaInN, GaInAsP, or the like. In other embodiments, the dopants may also include mixtures of Group II and Group VI elements. For example, the dopant may include mixtures of ZnO, ZnS, ZnSe, ZnTe, CdS, CdSe, CdTe, HgS, HgSe, HgTe, BeS, BeSe, BeTe, MgS, MgSe, or the like. Alloys or mixtures of these dopants are also be possible, for example, ZnCd Se, or ZnSSe or the like. Additionally, mixtures of different groups of semiconductors may also be possible, for example, combinations of Group II-Group VI and Group III-Group V elements, such as $(GaAs)_x(ZnS)_{1-x}$. Other non-limiting examples of dopants may include mixtures of Group IV and Group VI elements, for example GeS, GeSe, GeTe, SnS, SnSe, SnTe, PbO, PbS, PbSe, PbTe, etc.. Other dopant mixtures may include mixtures of Group I elements and Group VII elements, such as CuF, CuCl, CuBr, CuI, AgF, AgCl, AgBr, AgI, or the like. Other dopant mixtures may include different mixtures of these elements, such as $BeSiN_2$, $CaCN_2$, $ZnGeP_2$, $CdSnAs_2$, $ZnSnSb_2$, $CuGeP_3$, $CuSi_2P_3$, Si_3N_4, Ge_3N_4, Al_2O_3, $(Al, Ga, In)_2(S, Se, Te)_3$, Al_2CO, $(Cu, Ag)(Al, Ga, In, Tl, Fe)(S, Se, Te)_2$ or the like.

As a particular non-limiting example, a p-type dopant may be selected from Group III, and an n-type dopant may be selected from Group V. For instance, a p-type dopant may include at least one of B, Al and In, and an n-type dopant may include at least one of P, As and Sb. For Group III-Group V mixtures, a p-type dopant may be selected from Group II, including one or more of Mg, Zn, Cd and Hg, or Group IV,

including one or more of C and Si. An n-type dopant may be selected from at least one of Si, Ge, Sn, S, Se and Te. It will be understood that the invention is not limited to these dopants, but may include other elements, alloys, or mixtures as well.

The nanoscale wire of the present invention may further include, in some cases, any organic or inorganic molecules. In some cases, the organic or inorganic molecules are polarizable and/or have multiple charge states. For example, the nanoscale wires may include gallium arsenide, gallium nitride, indium phosphide, germanium, or cadmium selenide.

In yet another set of embodiments, nanoscale wire (or other nanostructured material) may comprise two or more regions having different compositions. One or more of the regions may include a metal-semiconductor compound. Each region of the nanoscale wire may have any shape or dimension, and these can be the same or different between regions. For example, a region may have a smallest dimension of less than 1 micron, less than 100 nm, less than 10 nm, or less than 1 nm. In some cases, one or more regions may be a single monolayer of atoms (i.e., "delta-doping"). In certain cases, the region may be less than a single monolayer thick (for example, if some of the atoms within the monolayer are absent).

The two or more regions may be longitudinally arranged relative to each other, and/or radially arranged (e.g., as in a core/shell arrangement) within the nanoscale wire. As one example, the nanoscale wire may have multiple regions of semiconductor materials arranged longitudinally. In another example, a nanoscale wire may have two regions having different compositions arranged longitudinally, surrounded by a third region or several regions, each having a composition different from that of the other regions. As a specific example, the regions may be arranged in a layered structure within the nanoscale wire, and one or more of the regions may be delta-doped or at least partially delta-doped. As another example, the nanoscale wire may have a series of regions positioned both longitudinally and radially relative to each other. The arrangement can include a core that differs in composition along its length (changes in composition or concentration longitudinally), while the lateral (radial) dimensions of the core do, or do not, change over the portion of the length differing in composition. The shell portions can be adjacent each other (contacting each other, or defining a change in composition or concentration of a unitary shell structure longitudinally), or can be separated from each other by, for example, air, an insulator, a fluid, or an auxiliary, non-

nanoscale wire component. The shell portions can be positioned directly on the core, or can be separated from the core by one or more intermediate shells portions that can themselves be constant in composition longitudinally, or varying in composition longitudinally. That is, the invention allows the provision of any combination of a nanowire core and any number of radially-positioned shells (e.g., concentric shells), where the core and/or any shells can vary in composition and/or concentration longitudinally, any shell sections can be spaced from any other shell sections longitudinally, and different numbers of shells can be provided at different locations longitudinally along the structure.

As used herein, regions that differ in composition may comprise different materials or elements, and/or may comprise the same materials or elements, but at different ratios or concentrations. Each region may be of any size or shape within the nanoscale wire. Two regions positioned adjacent to each other define a junction therebetween. A junction within the nanoscale wire may be, for example, a p/n junction, a p/p junction, an n/n junction, a p/i junction (where i refers to an intrinsic semiconductor), an n/i junction, an i/i junction, or the like. The junction may also be a Schottky junction. The junction may also be a semiconductor/semiconductor junction, a semiconductor/metal junction, a semiconductor/insulator junction, a metal/metal junction, a metal/insulator junction, an insulator/insulator junction, or the like. The junction may also be a junction of two materials, a doped semiconductor to a doped or an undoped semiconductor, or a junction between regions having different dopant concentrations. The junction may also be a defected region to a perfect single crystal, an amorphous region to a crystal, a crystal to another crystal, an amorphous region to another amorphous region, a defected region to another defected region, an amorphous region to a defected region, or the like. More than two regions may be present within the nanoscale wire, and these regions may have unique compositions, or may comprise the same compositions. As one example, a wire may have a first region having a first composition, a second region having a second composition, and a third region having a third composition or the same composition as the first composition.

The regions of the nanoscale wire may be distinct from each other with minimal cross-contamination, or the composition of the nanoscale wire may vary gradually from one region to the next. In some embodiments, the junction between two differing regions (e.g., between different longitudinal regions between a core and shell, between

two different shells, etc.) may be "atomically-abrupt," where there is a sharp transition at the atomic scale between two adjacent regions that differ in composition. However, in other embodiments, the junction between two differing regions may be more gradual. For example, the "overlap region" between the adjacent regions may be a few nanometers wide, for example, less than about 500 nm, less than about 100 nm, less than about 50 nm, less than about 40 nm, less than about 20 nm, or less than about 10 nm. In certain instances, the overlap region between a first region having a composition and a second region having a composition different from the first region (i.e., different concentrations or different species) can be defined as the distance between where the composition of the overlap region ranges between about 10 vol% and about 90 vol% of the composition of the first region, with the remainder having a complementary amount of the composition of the second region. In certain embodiments of the invention, nanoscale wires having more than one junction between two regions having different compositions are also contemplated. For example, a nanoscale wire may have two, three, four, or more overlap regions. The number of periods and the repeat spacing may be constant or varied.

In some embodiments, a gradual change in composition between two adjacent regions may relieve strain and may enable defect-free junctions and superlattices. However, in other embodiments, atomically-abrupt interfaces may be desirable, for example, in certain photonic and electronic applications. The nature of the interface between the two adjacent regions may be controlled by any suitable method (as further described below), for example, by using different nanocluster catalysts or varying the growth temperature when reactants are switched during synthesis. Nanoscale wires having atomically-abrupt regions may be fabricated, for example, by reducing the diameter of the nanoscale wire by reducing the size of the starting nanocluster, or by controlling exposure of the growing wire to dopant gases, for example, by selectively purging or evacuating the region surrounding the wire between different gas exposures or reaction conditions.

If the nanoscale wire includes one or more shells, the shells can be of the same or different composition relative to each other, and any of the shells can be of the same composition of a segment of the core, or of a different composition, or can contain the same or different concentration of a dopant as is provided in a section of the core. The shells may be grown using any suitable growth technique, for example, including the

techniques described herein, such as CVD or LCG. The shells and/or cores of the nanoscale wires may be etched using any suitable technique, including the techniques described herein. As one example, in a nanoscale wire having a shell and a core region different from the shell region, after being assembled on a substrate, the shell may be selectively etched off from the nanoscale wire or chemically reacted on the nanoscale wire.

In another aspect, the present invention contemplates a wide variety of devices. Such devices may include electrical devices, optical devices, optronic devices, spintronic devices, mechanical devices or any combination thereof, for example, optoelectronic devices or electromechanical devices. Functional devices assembled from the nanoscale wires (or other nanostructured materials) described herein may be used to produce various computer or device architectures. For example, certain nanoscale wires described herein, such as those including one or more metal-semiconductor compounds, may be assembled into nanoscale versions of conventional semiconductor devices, such as diodes, light emitting diodes (LEDs), inverters, sensors, bipolar transistors, etc. These devices may include single, free-standing nanoscale wires, crossed nanoscale wires, or combinations of single nanoscale wires combined with other components. Nanoscale wires having different dopants, doping levels, or combinations of dopants may also be used in certain cases to produce these devices. The nanoscale wires, in particular cases, may also have multiple regions, each of which may have different compositions, as previously described. In some embodiments, a further step may include the fabrication of these structures within the nanoscale wires themselves, wherein a single nanoscale wire is able to operate as a functional devices. In other embodiments, a nanoscale wire may also be used as an interconnect between two devices, or between a device and an external circuit or system.

The present invention, in one set of embodiments, includes the ability to fabricate essentially any electronic device from adjacent n-type and p-type semiconducting components. This includes any device that one of ordinary skill in the art would desirably make using n-type and p-type semiconductors in combination. Examples of such devices include, but are not limited to, field effect transistors (FETs), bipolar junction transistors (BJTs), tunnel diodes, modulation doped superlattices, complementary inverters, light emitting devices, light sensing devices, biological system imagers, biological and chemical detectors or sensors, thermal or temperature detectors,

Josephine junctions, nanoscale light sources, photodetectors such as polarization-sensitive photodetectors, gates, inverters, AND, NAND, NOT, OR, XOR, and NOR gates, latches, flip-flops, registers, switches, clock circuitry, static or dynamic memory devices and arrays, state machines, gate arrays, and any other dynamic or sequential logic or other digital devices including programmable circuits. Also included are analog devices and circuitry, including but not limited to, amplifiers, switches and other analog circuitry using active transistor devices, as well as mixed signal devices and signal processing circuitry. Also included are p/n junction devices with low turn-on voltages, p/n junction devices with high turn-on voltages, and computational devices such as a half-adder. Furthermore, junctions having large dielectric contrasts between two regions may be used to produce 1D waveguides with built-in photonic band gaps, or cavities for nanoscale wire lasers. In some embodiments, the nanoscale wires of the present invention may be manufactured during the device fabrication process. In certain cases, nanoscale wires of the present inventions may first be synthesized, then assembled in a device.

In one embodiment, the invention includes a nanoscale inverter. In some cases, the inverter may be constructed using adjacent regions having different compositions, for example, a p-type and an n-type semiconductor region. For example, in one embodiment, the invention provides a lightly-doped complementary inverters (complementary metal oxide semiconductors) arranged by contact of an n-type semiconductor region with a p-type semiconductor region. The invention also provides lightly-doped complementary inverters (complementary metal oxide semiconductors) arranged by contact of an n-type semiconductor with a p-type semiconductor, for example, by arrangement of crossed n-type and p-type semiconducting nanoscale wires, or by the arrangement of two adjacent regions.

The invention includes a nanoscale diode according to another embodiment. In some cases, the invention provides a diode constructed using adjacent regions having different compositions, for example, a p-type and an n-type semiconductor region, for example, Zener diodes, tunnel diodes, light-emitting diodes, and the like. For example, the diode may be a tunnel diodes heavily-doped with semiconducting components. A tunnel diode may be arranged similarly or exactly the same as a complementary inverter, with the semiconductors being heavily doped rather than lightly doped.

In yet another embodiment, the invention comprises a nanoscale transistor, such as a field effect transistor ("FET") or a bipolar junction transistor ("BJT"). The transistor may have a smallest width of less than 500 nm, less than 100 nm, or any other width as described herein. In one set of embodiments, the transistor may be constructed using adjacent regions having different compositions. As an example, a p-type and an n-type semiconductor region may be contemplated, for example, arranged longitudinally within a single wire, arranged radially within the wire, between adjacent crossed wires, and the like, as well as combinations of these. In some embodiments, the transistor may comprise a doped semiconductor, such as a p-type or n-type semiconductor, as is known by those of ordinary skill in the art in transistor fabrication. The present invention, in some cases, also contemplates controlled doping of nanoscale wires such that a fabrication process can involve fabricating functional FETs according to a technique in which much greater than one in fifty devices is functional. For example, the technique can involve preparing a doped nanoscale wire and fabricating an FET therefrom.

A FET comprising a nanoscale wire may serve as a conducting channel in some cases, and an elongated material having a smallest width of less than 500 nm (e.g., a nanoscale wire) serving as the gate electrode. For such a FET, the widths of the nanoscale wire and the elongated material may define a width of the FET. The field effect transistor may also, in some instances, comprise a doped or intrinsic semiconductor having at least one portion having a smallest width of less then 500 nanometers, and a gate electrode comprising an elongated material having at least one portion having a smallest width of less then 500 nanometers. Furthermore, in some cases, the nanoscale wire may comprise a semiconductor, and/or have a core/shell arrangement, and such a shell may function as a gate dielectric for the FET. In certain instances, the two regions may be longitudinally positioned. In certain cases, the intersection of a nanoscale wire and an elongated material may define a length of the FET. The transistor may also be a coaxially-gated transistor in some cases. In some cases, the FETs are readily integratable into devices, and the assembly of such FETs may be shrunk in a straightforward manner into nanometers scale. Such a "bottom-up" approach may scale down to sizes far beyond what is predicted for traditional "top-down" techniques typically used in the semiconductor industry today. Further, such bottom-up assembly may prove to be cheaper than the traditional top-down approach.

In another set of embodiments, various electronic devices incorporating the nanoscale wires of the invention may be controlled, for example, using any input signal, such as an electrical, optical or a magnetic signal. The control may involve switching between two or more discrete states, or may involve continuous control of nanoscale wire current, i. e., analog control. In addition to electrical signals, optical signals and magnetic signals, the devices may also be controlled in certain embodiments in response to biological and chemical species, for example, DNA, protein, metal ions, peptides, etc. Any species that is charged or has a dipole moment may be detected in some cases. In other embodiments, the device may be switchable in response to mechanical stimuli, for example, mechanical stretching, vibration and bending. In yet other embodiments, the device may be switchable in response to an external physical stimulus such as temperature, pressure, or fluid movement, for example, the movement of an environmental gas or liquid.

In yet another set of embodiments, devices including nanoscale wires having more than one region able to produce or emit light are contemplated. For example, a nanoscale wire having multiple p-type and n-type regions which may be produced, where each p/n junction is able to emit light. The nanoscale wire may have two, three, four, five, or more p/n junctions. The number of periods and the repeat spacing between each p/n junction may be constant or varied during growth. Thus, for example, nanoscale wires having multiple light-emitting and non-light-emitting regions may be used as "nano-bar codes," where different sequences, patterns, and/or frequencies of light-emitting and non-light-emitting regions may be used to uniquely "tag" or label an article that the nanoscale wire is used in. Varying the composition of each p/n junction (for example, by using different dopants) may alter the frequency of the emitted light; thus, additional information can be encoded through variations in the color of the emitting region using multi-component superlattices in certain instances.

In still another set of embodiments, a device including nanoscale wire may be used as a photodetector. In some cases, the responsivity of the nanophotodetector may be greater than about 1000 A/W, greater than about 3000 A/W, still greater than about 5000 A/W, or greater than about 10000 A/W. In certain embodiments, the response time of the semiconductor photodetector may be less than 1 ps, less than about 100 fs, less than about 10 fs, or still less than about 1 fs, due to the small capacitances of the nanoscale wires, which may be less than about 100 aF or about 10 aF in some cases.

Electrically erasable and re-writable memory structures and devices with reversible states and good retention time may be constructed using the nanoscale wires of the invention, according to another set of embodiments. When the surfaces of these devices are appropriately modified with either molecules or nanocrystals, reversible memory switching behavior may be observed when electrical pulses of opposite polarity is applied. Specifically, subjection to positive or negative voltage pulses in either gate or bias voltages may cause the devices to make fully reversible transition between low-resistance and high resistance states. In some cases, the transition between states is performed directly, through the flow of electrons through the device or component. In other cases, the transition between states is accomplished inductively, through the use of field effects, electron tunneling, or the like.

In some cases, nanoscale memory switching device may be assembled from one or more nanoscale wires described herein. The memory switching device may have multiple states, non-volatile reversible states, or a large on/off ratio in some instances. The nanoscale memory switching devices may be highly parallel and scalable with simple chemical assembly process, and can be useful in construction of a chemically assemble computer in some embodiments.

The memory switching device, in one embodiment, is a three terminal devices based on individual nanoscale wires using the gate pulse to induce the switching between two states, such as between high- and low-resistance states. In another embodiment, the memory switching device is a two terminal devices based on individual nanoscale wires using the bias pulse to induce the switching between high- and low-resistance states. In yet another embodiment, the memory switching device is based on the junction between two regions having different compositions, for example, in a core/shell arrangement, in an arrangement where the two regions are longitudinally positioned relative to each other, in arrangements having crossed nanoscale wire p-n junctions, etc. A bias pulse or a gate pulse may be used to induce switching between high- and low resistance states, for example, by supplying a charge or a current through the nanoscale wire or a region thereof, such as through a core region. In still another embodiment, the memory switching device may have three, four, six, eight, or other multiple states or configurations.

In some cases, memory systems using the nanoscale wires of the invention may take the form of novel structures such as two-dimensional parallel, crossing, or three-

dimensional stacked memory arrays to achieve ultra-high density data storage, and non-volatile state switches for computer systems fabricated by chemical assembly. Thus, it is possible to achieve an active element two-dimensional density of at least 10^{11} memory elements/cm^2, preferably at least about 10^{12} memory elements/cm^2. For example, using nanoscale wires of 10 micron length, with a memory element every 20 nm along each nanoscale wire, an array can be formed with 500 parallel wires in each direction, each wire containing 500 crossbar array junctions (memory elements). For instance, 250,000 memory elements may be formed in such an array. Three-dimensional arrays can be created as well, in some instances. For example, where a 1 micron spacing is created between two-dimensional array planes, the invention provides a three-dimensional array density of at least about 10^{14} memory elements/cm^3, and in some cases, at least about 10^{15} memory elements/cm^3 or more.

The invention, in yet another set of embodiments, provides a sensing element. The sensing element may be an electronic sensing element, and the sensing element may include a nanoscale wire able to detect the presence, absence, and/or amount (concentration), of a species such as an analyte in a sample (e.g. a fluid sample) containing, or suspected of containing, the species. Nanoscale sensors of the invention may be used, for example, in chemical applications to detect pH or the presence of metal ions; in biological applications to detect a protein, nucleic acid (e.g. DNA, RNA, etc.), a sugar or carbohydrate, and/or metal ions; and in environmental applications to detect pH, metal ions, or other analytes of interest. Also provided, according to another embodiment, is an article comprising a nanoscale wire and a detector constructed and arranged to determine a change in an electrical property of the nanoscale wire. At least a portion of the nanoscale wire is addressable by a sample containing, or suspected of containing, an analyte. The phrase "addressable by a fluid" is defined as the ability of the fluid to be positioned relative to the nanoscale wire so that an analyte suspected of being in the fluid is able to interact with the nanoscale wire. The fluid may be proximate to or in contact with the nanoscale wire.

The nanoscale wire, in certain cases, may be chosen on the basis of its ability to interact with an analyte, i.e., whether the appropriate reaction entity, e.g. a binding partner, can be easily attached to the surface of the nanoscale wire, and/or whether the appropriate reaction entity, e.g. a binding partner, can be positioned near the surface of the nanoscale wire. The selection of suitable nanostructures, e.g., conductors or

semiconductors, nanotubes or nanoscale wires, will be apparent and readily reproducible by those of ordinary skill in the art with the benefit of the present disclosure. The term "binding partner," as used herein, refers to a molecule that can undergo binding with a particular molecule. Biological binding partners are examples. Non-limiting examples include nucleic acid-nucleic acid binding, nucleic acid-protein binding, protein-protein binding, enzyme-substrate binding, receptor-ligand binding, receptor-hormone binding, antibody-antigen binding, etc.

In some cases, chemical changes associated with a nanoscale wires can be used to modulate the properties of the nanoscale wires to create electronic devices of a variety of types. The presence of an analyte can change the electrical properties of the nanoscale wires, e.g., through electrocoupling with a binding agent of the nanoscale wire. If desired, the nanoscale wires may be coated with a specific reaction entity, binding partner or specific binding partner, chosen for its chemical or biological specificity to a particular analyte.

The reaction entity may be positioned relative to the nanoscale wire to cause a detectable change in the nanoscale wire. In some cases, the reaction entity may be positioned within 100 nm of the nanoscale wire, within 50 nm of the nanoscale wire, or within 10 nm of the nanoscale wire. The actual proximity can be determined by those of ordinary skill in the art. In one embodiment, the reaction entity is positioned less than 5 nm from the nanoscopic wire. In other embodiments, the reaction entity is positioned with 4 nm, 3 nm, 2 nm, and 1 nm of the nanoscopic wire. In one embodiment, the reaction entity is attached to the nanoscopic wire through a linker.

The invention, in another embodiment, provides an article comprising a sample exposure region and a nanoscale wire able to detect the presence or absence of an analyte, and/or the concentration of the analyte. The sample exposure region may be any region in close proximity to the nanoscale wire wherein a sample in the sample exposure region addresses at least a portion of the nanoscale wire. Examples of sample exposure regions include, but are not limited to, a well, a channel, a microchannel, and a gel. In certain embodiments, the sample exposure region is able to hold a sample proximate the nanoscale wire, and/or may direct a sample toward the nanoscale wire for determination of an analyte in the sample. The nanoscale wire may be positioned adjacent to or within the sample exposure region. Alternatively, the nanoscale wire may be a probe that is inserted into a fluid or fluid flow path. The nanoscale wire probe may also comprise a

microneedle and the sample exposure region may be addressable by a biological sample. In this arrangement, a device that is constructed and arranged for insertion of a microneedle probe into a biological sample will include a region surrounding the microneedle that defines the sample exposure region, and a sample in the sample exposure region is addressable by the nanoscale wire, and vice versa. Fluid flow channels can be created at a size and scale advantageous for use in the invention (microchannels) using a variety of techniques such as those described in International Patent Publication No. WO 97/33737, published September 18, 1997, and incorporated herein by reference.

In yet another aspect, the present invention provides a method of preparing a nanostructure. In one set of embodiments, the method involves allowing a first material to diffuse into at least part of a second material, optionally creating a new compound. In some cases, diffusion may proceed until at least part of the first material reaches a center portion of the first material, or until the first material has been incorporated substantially throughout the second material (e.g., the second material has been "bulk-doped" with the first material). The first and second materials may each be metals or semiconductors, one material may be a metal and the other material may be a semiconductor, etc. Diffusion of the first material in the second material may occur, in one set of embodiments, passively or spontaneously, i.e., no external conditions may be necessary to cause the first material to diffuse into the second material. In another set of embodiments, diffusion of the first material into the second material may occur under external conditions related to those involved in the formation and/or positioning of the first and/or second materials. In yet another set of embodiments, the first material may be unable to diffuse into the second material under normal or ambient conditions (for example, under room temperature and/or pressure), or under conditions involved in the formation and/or positioning of the first and/or second materials, but diffusion of the first material into the second material may be initiated and/or facilitated by the application of suitable external conditions able to promote diffusion, for example, increases in temperature and/or pressure. In still another set of embodiments, diffusion of the first material into the second material may be initiated by applying an external stimulus, for example, by altering the temperature and/or pressure, by removing an intervening layer positioned between the first material and the second material, or the like. It should be understood that "diffuse," as used herein, refers to diffusion processes

that occurs on detectable time scales of interest, e.g., the migration of the atoms of a first material into a second material on the nanoscale may be detectable within about an hour, using techniques known to those of ordinary skill in the art (for example, electron or optical microscopy, measurements of resistivity or conductivity, etc.). In many cases, the migration of the atoms of the first material into the second material may be detected within about 30 minutes, within about 15 minutes, within about 10 minutes, or within about 5 minutes. Thus, as an example, diffusion may be allowed to proceed until the conductivity of the second material has been substantially altered, for instance, such that the conductivity of the second material has been altered from that of a semiconductor to that of a conductor (or vice versa), etc.

The nanostructure, after the first material has diffused into at least part of the second material, may have any of the structures described herein, for example, a single crystal wire, a wire comprising a core/shell heterojunction, a wire comprising a longitudinal heterojunction, a device comprising a wire, or the like. The materials for the nanostructure may be chosen such that the diffusing material is able to diffuse into at least an interior portion of the receiving material, i.e., internally of the surface of the receiving material. The method, in some cases, may be used to prepare a nanostructure comprising a metal-semiconductor compound such as a metal silicide. One or more of any of the following-described methods may also be used in the preparation of a nanostructure comprising a metal-semiconductor compound.

In one embodiment, a first material is positioned adjacent or proximate to a second material (by known forms of deposition, for example), and the atoms of the first material are allowed to diffuse into at least a portion of the second material. At least one of the first and second materials may be a nanoscale material. Thus, as an example, in Fig. 5A, a first material 51 is positioned next to a second material 52. The first material may be positioned such that it contacts the second material, and/or such that atoms from the first material are able to diffuse into the second material (for example, an intervening material or space may be present between the first material and the second material). Diffusion of the first material into at least a portion of the second material is then allowed to occur, as shown in Fig. 5B. When sufficient diffusion has occurred (i.e., when a desired amount of the first material has diffused into the second material), the first material (or at least a portion thereof) may optionally be removed, as is shown in Fig. 5C.

For example, to create a nanoscale wire comprising a metal-semiconductor compound, a metal may be positioned adjacent or proximate to a semiconductor (by known forms of deposition, for example), and the metal atoms allowed to diffuse into at least a portion of the semiconductor material, for example, to create one or more heterojunctions within the nanoscale wire. The metal may be a bulk metal in some cases, i.e., a metal having a volume of at least nanoscopic dimensions (e.g., having a smallest dimension of at least about 1 nm).

In some cases, diffusion of the metal atoms into the semiconductor may be initiated and/or facilitated, for example, by the application of high pressures and/or high temperatures, for example, temperatures of at least about 500°C, at least about 550°C, at least about 600°C, at least about 700°C, or more in some cases. In certain instances, substantial diffusion of metal atoms into the semiconductor may not substantially occur absent an increase or an alteration in the temperature and/or pressure. In some cases, diffusion of the metal atoms into the semiconductor (or at least a portion thereof) may proceed until a metal-semiconductor compound forms (e.g., through a chemical reaction), and/or when a stoichiometric ratio of metal atoms to semiconductor atoms has been established. As a particular example, if the metal is a transition metal such as nickel, and the semiconductor material is silicon nanoscale wire, diffusion of nickel into the silicon nanoscale wire may proceed until the silicon nanoscale wire (or at least that portion of the nanoscale wire exposed to nickel) has been converted into a nickel silicide nanoscale wire. In other cases, however, the metal atoms and the semiconductor atoms may not be in a stoichiometric ratio. In certain instance, diffusion of the metal into the semiconductor may be stopped before metal-semiconductor compound formation or stoichiometric equilibrium has been established, thus, in one embodiment, the nanoscale wire may include a non-stoichiometric ratio of metal atoms to semiconductor atoms.

After the metal atoms have been allowed to diffuse into the semiconductor, in some cases, excess metal may be removed from the semiconductor, for example, by the application of certain species such as metal etchants. For example, if the metal diffused into the semiconductor is nickel, a suitable metal etchant may include acids such as nitric acid, sulfuric acid, hydrochloric acid, and/or nickel etchants such as TFB or TFG (available from Transene, Danvers, MA). In some cases, the removal of the excess metal from the semiconductor may be facilitated by elevated temperatures and/or pressures.

In another set of embodiments, a nanostructure can be prepared by exposing a portion of the second material to the first material. The first material can diffuse into regions of the second material that are adjacent or proximate the first material, while regions of the second material not adjacent or proximate the first material will remain substantially free of the first material. As one example, as shown in Fig. 3A, a mask 38 may be patterned on a nanostructure 37 (or other nanostructure) to define one or more regions where the nanostructure is covered by the mask 60 and one or more regions where the nanostructure is free of the mask 65. The mask may have any pattern defined therein, and can define 2- or 3-dimensional patterns on the nanostructure, depending on the specific application. Any suitable material may be used to form the mask, for instance, a photoresist may be formed on the nanostructure to define a mask, e.g., through photolithographic techniques known to those of ordinary skill in the art. As a non-limiting example, a mask with a series of openings may be formed on a nanowire to create a series of heterojunctions along the nanowire, or if not formed on the nanowire (or other nanostructure), positioned in proximity relative to the nanowire so as to be able to mask application of material on the nanowire. As another example, a mask may be formed from a nanoscale wire, for example, a nanoscale wire, a nanotube, a core/shell nanoscale wire, etc. For instance, the nanoscale wire used as a mask may be placed on or positioned in proximity to the nanowire (or other nanostructure); the nanoscale wire used as a mask may thus mask application of material on the nanowire.

After positioning of the mask on the second material of the nanostructure, or between the nanostructure and the source of material to be deposited thereto, the first material may be deposited on the mask. Regions of the nanostructure that are free of the mask 65 will have the first material deposited thereon, while regions of the nanostructure covered by the mask 60 will not be exposed to the first material. The first material can then diffuse into the portions second material adjacent or proximate the first material. The mask may be removed before or after diffusion of the first material into portions of the second material. After diffusion, a nanostructure having one or more heterojunctions 67, defined by the mask, can be created.

In yet another set of embodiments, the present invention involves controlling and altering the doping of semiconductors in a nanoscale wire. In some cases, the nanoscale wires (or other nanostructure) may be produced using techniques that allow for direct and controlled growth of the nanoscale wires. For instance, the direct growth of doped

nanoscale wires may eliminate the need to use lithographic steps during production of the nanoscale wire, thus facilitating the "bottom-up" assembly of complex functional structures. Fabrication paradigms for single nanoscale wire devices that are contemplated in the present invention include, but are not limited to, direct fabrication of nanoscale wire junctions during synthesis, or doping of nanoscale wires via post-synthesis techniques (e. g., annealing of dopants from contacts or solution-processing techniques). The dopants may be changed at any point during the growth of the nanoscale wire.

In some cases, the nanoscale wire may be doped during growth of the nanoscale wire. Doping the nanoscale wire during growth may result in the property that the doped nanoscale wire is bulk-doped. Furthermore, such doped nanoscale wires may be controllably doped, such that a concentration of a dopant within the doped nanoscale wire can be controlled and therefore reproduced consistently, making possible the commercial production of such nanoscale wires. Additionally, the dopant may be systematically altered during the growth of the nanoscale wire, for example, so that the final nanoscale wire has a first doped region comprising a first dopant and a second doped region differing in composition from the first region, for example, by comprising a second dopant, comprising the first dopant at a different concentration, or omitting the first dopant.

Certain embodiments of the invention may utilize metal-catalyzed CVD techniques ("chemical vapor deposition") to synthesize individual nanoscale wires. CVD synthetic procedures useful for preparing individual wires directly on surfaces and in bulk form are generally known, and can readily be carried out by those of ordinary skill in the art. See, for example, Kong, *et al.*, "Synthesis of Individual Single-Walled Carbon Nanotubes on Patterned Silicon Wafers," *Nature*, 395:878-881 (1998); or Kong, *et al.*, "Chemical Vapor Deposition of Methane for Single-Walled Carbon Nanotubes," *Chem. Phys. Lett.*, 292:567-574 (1998). Nanoscopic wires may also be grown through laser catalytic growth. See, for example, Morales, *et al.*, "A Laser Ablation Method for the Synthesis of Crystalline Semiconductor Nanowires," *Science*, 279:208-211 (1998). With the same basic principles as LCG, if uniform diameter nanoclusters (less than 10-20% variation depending on how uniform the nanoclusters are) are used as the catalytic cluster, nanoscale wires with uniform size (diameter) distribution can be produced, where the diameter of the nanoscale wires is determined by the size of the catalytic

clusters. By controlling the growth time, nanoscale wires with different lengths can be grown.

One technique that may be used to grow nanoscale wires is catalytic chemical vapor deposition ("C-CVD"). In the C-CVD method, the reactant molecules are formed from the vapor phase, as opposed to from laser vaporization. In C-CVD, nanoscale wires may be doped by introducing the doping element into the vapor phase reactant (e. g. diborane and phosphane for p-type and n-type doped regions). The doping concentration may be controlled by controlling the relative amount of the doping compound introduced in the composite target. The final doping concentration or ratios are not necessarily the same as the vapor-phase concentration or ratios. By controlling growth conditions, such as temperature, pressure or the like, nanoscale wires having the same doping concentration may be produced. To produce a nanoscale wire having adjacent regions having different compositions within a nanoscale wire, the doping concentration may be varied by simply varying the ratio of gas reactant (e. g. from about 1 ppm to about 10%, from about 10 ppm to about 20%, from about 100 ppm to about 50%, or the like), or the types of gas reactants used may be altered during growth of the nanoscale wire. The gas reactant ratio or the type of gas reactants used may be altered several times during growth of the nanoscale wire, which may produce nanoscale wires comprising regions having multiple compositions, all of which may or may not be unique.

Another technique for direct fabrication of nanoscale wire junctions during synthesis is generally referred to as laser catalytic growth ("LCG"). In laser catalytic growth, dopants are controllably introduced during vapor phase growth of nanoscale wires. Laser vaporization of a composite target composed of a desired material (e. g. silicon or indium phosphide) and a catalytic material (e. g. a nanoparticle catalyst) may create a hot, dense vapor. The vapor may condenses into liquid nanoclusters through collision with a buffer gas. Growth may begin when the liquid nanoclusters become supersaturated with the desired phase and can continue as long as reactant is available. Growth may terminate when the nanoscale wire passes out of the hot reaction zone or when the temperature is decreased. The nanoscale wire may be further subjected to different semiconductor reagents during growth.

The catalytic materials and/or the vapor phase reactants may be produced by any suitable technique. For example, laser ablation techniques may be used to generate catalytic clusters or vapor phase reactant that may be used during LCG. Other

techniques are also contemplated, such as thermal evaporation techniques. The laser ablation technique may generate liquid nanoclusters that may subsequently define the size and direct the growth direction of the nanoscopic wires. The diameters of the resulting nanoscale wires may be determined by the size of the catalyst cluster, which in turn may be determined using routine experiments that vary the growth conditions, such as background pressure, temperature, flow rate of reactants, and the like. For example, lower pressure generally produces nanoscale wires with smaller diameters. Further diameter control may be achieved by using uniform diameter catalytic clusters.

As an example, vapor phase semiconductor reactants required for nanoscale wire growth may be produced by laser ablation of solid targets, vapor-phase molecular species, or the like. Any catalyst able to catalyze the production of nanoscale wires may be used. Gold may be preferred in certain embodiments. A wide range of other materials may also be contemplated, for example, a transition metal such as silver, copper, zinc, cadmium, iron, nickel, cobalt, and the like. Generally, any metal able to form an alloy with the desired semiconductor material, but does not form a more stable compound than with the elements of the desired semiconductor material may be used as the catalyst. The buffer gas may be any inert gas, for example, N_2 or a noble gas such as argon. In some embodiments, a mixture of H_2 and a buffer gas may be used to reduce undesired oxidation by residual oxygen gas.

A reactive gas used during the synthesis of the nanoscale wire may also be introduced when desired, for example, ammonia for semiconductors containing nitrogen. Nanoscale wires may also be flexibly doped by introducing one or more dopants into the composite target, for example, a germanium alloy during n-type doping of InP. The doping concentration may be controlled by controlling the relative amount of doping element, for example, between 0 and about 10% or about 20%, introduced in the composite target.

Laser ablation may generate liquid nanoclusters that subsequently define the size and direct the growth direction of the nanoscale wires. The diameters of the resulting nanoscale wires are determined by the size of the catalyst cluster, which may be varied by controlling the growth conditions, such as the pressure, the temperature, the flow rate and the like. For example, lower pressure may produce nanoscale wires with smaller diameters in certain cases. Further diameter control may be performed by using uniform diameter catalytic clusters.

If substantially uniform diameter nanoclusters (less than 10% to 20% variation depending on how uniform the nanoclusters are) are used as the catalytic material, nanoscale wires with substantially uniform size (diameter) distribution can be produced, where the diameter of the nanoscale wires generally is determined by the size of the catalytic material. By controlling the growth time or the position of the sample within the reactor, nanoscale wires with different lengths or different shell thicknesses may be grown.

To create a single junction within a nanoscale wire, in one set of the embodiments, the addition of the first reactant may be stopped during growth, and then a second reactant may be introduced for the remainder of the synthesis. This can be done abruptly, or a gradual change between reactants can be made, to result in an abrupt or gradual junction. Repeated modulation of the reactants, optionally with different reactants, during growth is also contemplated, which may produce nanoscale wire superlattices. LCG also may require a nanocluster catalyst suitable for growth of the different super lattice components, for example, a gold nanocluster catalyst can be used in a wide range of metal-semiconductor nanoscale wires, as well as Group III-V and Group IV materials. Substantially monodisperse metal nanoclusters may be used to control the diameter, and, through growth time, the length various semiconductor nanoscale wires.

As another example, LCG methods may be used to create nanoscale wires having a multishell configuration. For example, by altering the synthetic conditions during laser catalytic growth, homogeneous reactant decomposition may occur on the surface of the nanoscale wire. Control of the synthetic conditions may lead to a shell forming on the surface of the nanoscale wire, and in some embodiments, the synthetic reaction conditions may be controlled to cause the formation of a thin, uniform shell, a shell having a thickness of one atomic layer, or less in some cases. In other embodiments, by modulating or altering the reactants within the laser catalytic growth system, more than one shell may be built up on the outer surface of the nanoscale wire. As one none limiting example, a nickel silicide nanoscale wire core may be grown, and additional semiconductor materials may be deposited onto the surface, for example, a germanium shell, or a silicon shell doped with a dopant such as boron, or other dopants as described elsewhere in this application. The boundaries between the shells may be atomically abrupt, or may be graduated in some fashion, depending on how reactants such as, for

example, silane, germane, or diborane are introduced into the laser catalytic growth system. Arbitrary sequences of Si, Ge, NiSi, and alloy overlayers on both Si and Ge nanowire cores may also be prepared. Thus, a nanoscale wire having a core/shell arrangement may comprise a metal-semiconductor compound such as a metal silicide in the core and/or in at least one shell, or both in some cases. Other factors may contribute to the growing nanoscale wire, such as, for example, the reaction temperature, or the sample position within the furnace. By varying these parameters, the ratio of axial growth to radio growth may be controlled as desired.

In some cases, this methodology allows the direct formation of adjacent regions having different compositions within a nanoscale wire, such as a p/n junction, and/or adjacent regions differing in concentration of a particular element or composition. LCG also allows the creation of semiconductor superlattices, in which multiple layers of different composition are grown, which may give rise to a one-dimensional analog of multiple quantum states that are well known from thin-film studies. Alteration of the semiconductor reagents may allow for the formation of abrupt or gradual changes in the composition of the growing semiconductor material, allowing heterostructured materials to be synthesized. One non-limiting example of an LCG-grown semiconductor is a NiSi/GaAs heterojunction, which includes an initial growth of NiSi, followed by subsequent GaAs growth, giving an abrupt junction within a single nanoscale wire.

Other techniques to produce nanoscale semiconductors such as nanoscale wires are also within the scope of the present invention. For example, nanoscale wires of any of a variety of materials may be grown directly from vapor phase through a vapor-solid process. Also, nanoscale wires may also be produced by deposition on the edge of surface steps, or other types of patterned surfaces. Further, nanoscale wires may be grown by vapor deposition in or on any generally elongated template. The porous membrane may be porous silicon, anodic alumina, a diblock copolymer, or any other similar structure. The natural fiber may be DNA molecules, protein molecules carbon nanotubes, any other elongated structures. For all the above described techniques, the source materials may be a solution or a vapor. In some embodiments, while in solution phase, the template may also include be column micelles formed by surfactant molecules in addition to the templates described above.

In some cases, the nanoscale wire may be doped after formation. In one technique of post-synthetic doping of nanoscale wires, a nanoscale wire having a

substantially homogeneous composition is first synthesized, then is doped post-synthetically with various dopants. Such doping may occur throughout the entire nanoscale wire, or in one or more portions of the nanoscale wire, for example, in a wire having multiple regions differing in composition. Thus, as a specific non-limiting example, a semiconductor nanoscale wire may be prepared, then one or more regions of the nanoscale wire may be exposed to a dopant, thus resulting in a semiconductor nanoscale wire having a series of undoped semiconductor regions and doped semiconductor regions. As another example, a p/n junction can be created by introducing p-type and an n-type dopants down onto a single nanoscale wire. The p/n junction can then be further annealed in some cases to allow the dopants to migrate further into the nanoscale wire to form a bulk-doped nanoscale wire.

The following U.S. provisional and utility patent applications are incorporated herein by reference in their entirety for all purposes: Serial No. 60/524,301, entitled, "Nanoscale Arrays and Related Devices," filed November 20, 2003; Serial No. 10/196,337, entitled, "Nanoscale Wires and Related Devices," filed July 16, 2002, published as Publication No. 2003/0089899 on May 15, 2003; Serial No. 10/152,490, entitled, "Nanoscale Wires and Related Devices," filed May 20, 2002; Serial No. 60/226,835, entitled, "Semiconductor Nanowires," filed August 22, 2000; Serial No. 60/254,745, entitled, "Nanowire and Nanotube Nanosensors," filed December 11, 2000; Serial No. 60/292,035, entitled "Nanowire and Nanotube Nanosensors," filed May 18, 2001; Serial No. 60/292,121, entitled, "Semiconductor Nanowires," filed May 18, 2001; Serial No. 60/292,045, entitled "Nanowire Electronic Devices Including Memory and Switching Devices," filed May 18, 2001; Serial No. 60/291,896, entitled "Nanowire Devices Including Emissive Elements and Sensors," filed May 18, 2001; Serial No. 09/935,776, entitled "Doped Elongated Semiconductors, Growing Such Semiconductors, Devices Including Such Semiconductors, and Fabricating Such Devices," filed August 22, 2001, published as Publication No. 20020130311 on September 19, 2002; Serial No. 10/020,004, entitled "Nanosensors," filed December 11, 2001, published as Publication No. 20020117659 on August 29, 2002; Serial No. 60/348,313, entitled "Transistors, Diodes, Logic Gates and Other Devices Assembled from Nanowire Building Blocks," filed November 9, 2001; Serial No. 60/354,642, entitled "Nanowire Devices Including Emissive Elements and Sensors," filed February 6, 2002; and Serial No. 60/544,800, entitled "Nanostructures Containing Metal-Semiconductor Compounds," filed February

13, 2004. The following International Patent Publications are incorporated herein by reference in their entirety for all purposes: Application Serial No. PCT/US01/26298, entitled "Doped Elongated Semiconductors, Growing Such Semiconductors, Devices Including Such Semiconductors, and Fabricating Such Devices," filed August 22, 2001, published as Publication No. WO 02/17362 on February 28, 2002; Application Serial No. PCT/US01/48230, entitled "Nanosensors," filed December 11, 2001, published as Publication No. WO 02/48701 on June 20, 2002; Application Serial No. PCT/US02/16133, entitled "Nanoscale Wires and Related Devices." filed May 20, 2002, published as Publication No. WO 03/005450 on January 16, 2003.

The following examples are intended to illustrate certain aspects of certain embodiments of the present invention, but do not exemplify the full scope of the invention.

EXAMPLE 1

This example illustrates the preparation of single-crystal NiSi nanowires, according to one embodiment of the invention. With reference to Fig. 1A, silicon nanowires were synthesized via chemical vapor deposition using monodisperse gold nanocluster catalysts (Ted Pella) as catalysts and silane (SiH_4) as vapor-phase reactant, using previously reported techniques (nanowire 11 in Fig. 1A). The nanowire was determined to have a substantially uniform diameter. Next, a growth wafer with free-standing silicon nanowires (e.g., nanowire 11) was loaded into a thermal evaporator after growth, then nickel metal having approximately the same thickness as the silicon nanowires diameter was evaporated onto the silicon nanowires (nanowire 12). After evaporation, nickel was allowed to diffuse into the silicon nanowires by annealing at 350-550 °C (nanowire 13). Depending on the temperature of the silicon nanowires, diffusion of nickel into the silicon nanowires occurs in under 1 hour, and often under 30 minutes. For instance, if the nanowires are heating using a tube furnace, diffusion of nickel into the nanowires occurred in approximately 30 minutes. Using rapid thermal annealing (RTA) or rapid thermal processing (RTP) techniques that can reach to 350-550 °C in a few seconds, diffusion of the nickel into the nanowires occurred in about 5 minutes.

The excess nickel was then removed by etchant (TFG, Transene Co.), followed by a post-annealing period at 600 °C. All of the annealing and post-annealing steps were

carried out in hydrogen gas for 30 minutes in a tube furnace or for 5 minutes using RTP/RTA techniques (nanowire 14).

EXAMPLE 2

This example illustrates the preparation of NiSi/Si nanowire heterostructures, according to another embodiment of the invention. With reference to Fig. 3A, silicon nanowires dispersed in ethanol were deposited on a semiconductor wafer with 600 nm oxide (substrate 31 in Fig. 3A). A photolithography process was used to define nickel silicide regions as follows (see substrate 32 in Fig. 3A). Shipley S1813 photoresist was deposited by spin coating onto the wafer. The photoresist was then exposed for about 2 seconds on an ABM photoaligner using a 1 micron line-width, 2 micron pitch) striped photomask to define the nickel silicide regions. After developing for approximately 1 min, the wafer was transferred to a thermal evaporator and nickel was evaporated onto the wafer with a thickness approximately equal to the diameter of the nanowire (substrate 32). After the evaporation and lift-off of excess photoresist, annealing, etching, and post-annealing were performed using techniques similar to those described in Example 1. This method yielded NiSi/Si nanowire heterostructures with a well-defined pattern determined by the line pattern of the photomask.

EXAMPLE 3

In this example, metallic nickel silicide nanowires were formed from semiconductor silicon nanowires and characterized. The preparation of nickel silicide (NiSi) nanowires in this example uses a simple solid-state reaction between nickel and silicon nanowires under annealing conditions, similar to those discussed in Example 1.

Fig. 1B shows a typical transmission electron microscopy (TEM) image of nanowires prepared from silicon nanowires grown from 20 nm gold nanoclusters. The nanowires have substantially uniform diameters (22.8 ± 3.4 nm) with lengths of nanometers up to several micrometers. Energy dispersive X-ray spectroscopy (EDS) measurements showed that the atom ratio between nickel and silicon in the nanowires was stoichiometric (%Ni:%Si = 1.03:1). The scale bar indicates 500 nm.

Figs. 1C and 1D illustrate representative high resolution transmission electron microscopy (HRTEM) images. In these images, the scale bar represents 5 nm. These images illustrate single-crystal nickel silicide nanowire structures. Fig. 1C is a HRTEM image of a 20 nm nickel silicide nanowire prepared using silicon nanowires grown from

20 nm gold nanoclusters. The growth front of the nanowire is in the $(1\bar{1}1)$ plane. A two-dimensional Fourier transform (inset, Fig. 1C) of the TEM image of the 20 nm nanowire depicts the $[10\bar{1}]$ zone axis of the nickel silicide wire. Fig. 1D is a HRTEM image of a 32 nm nickel silicide nanowire prepared using silicon nanowires grown from 30 nm gold nanoclusters. The high yield of nickel silicide nanowires with single crystallinity extended from the controlled growth of silicon nanowire allowed additional characterization of their physical properties, as discussed below. The growth front of the nanowire is in the (001) plane. The inset of Fig. 2D shows a two-dimensional Fourier transform of the image depicting the $[2\bar{1}0]$ zone axis of the nickel silicide.

EXAMPLE 4

In this example, certain transport properties of single-crystal nickel silicide nanowires were characterized. Two-terminal and four-terminal transport measurements were performed on individual nickel silicide nanowires, fabricated using techniques similar to those described in Example 1. All of the more than 100 nanowires used in this example showed a linear I-V response and a two-probe resistance of about 1 to about 5 kOhm (kΩ). While a simple calculation using the bulk resistivity of about 10 microOhm cm (μΩ cm) for single-crystal nickel silicide nanowires gave resistances of about 80 Ohms (Ω) to about 480 Ohms for each nanowire having diameters from 20 nm to 50 nm and a conducting channel length of around 1.5 microns in these experiments, the contact resistance between the chromium/gold electrode used and the nanowires may contribute a large proportion to the total resistance measured.

As confirmation, the four-probe experiments showed that among these resistances, the true resistance of nickel silicide nanowires only accounts for less than about 50% of the measured resistance, as illustrated in Fig. 2A. This figure illustrates current vs. voltage curves of a 29 nm nickel silicide nanowire with linear responses, with curve 20 corresponding to two-terminal measurement result and curve 25 corresponding to four-terminal measurement result. In this figure, the two-probe resistance was found to be about 890 Ohm, while the true resistance of a 29 nm diameter nickel silicide nanowire was determined to be about 180 Ohm using the four-probe method, corresponding to a resistivity of about 9.2 microOhm cm (μΩ cm).

The four-probe study, performed on more than 30 nanowires with diameters of about 18 nm to about 50 nm, gave resistivities of between about 6 microOhm cm and

about 60 microOhm cm. The inset in Fig. 2A is a scanning electron microscopy (SEM) image of the 29 nm NiSi four-terminal device. The scale bar in Fig. 2A represents 1 micron. Resistivity values of larger than 10 microOhm cm were believed to be due to defects in some samples, which can be eliminated by optimizing the fabrication process, using routine techniques known to those of ordinary skill in the art. The similarity between the measured true resistivity and bulk value suggested that a diffusive transport of charge carriers is responsible and the resistivity does not rise as the sizes of our nanowires decreases.

Temperature-dependent measurements further demonstrate that the resistance of the nanowires decreases approximately linearly with temperatures from about 300 K to about 60 K, further confirming the metallic behavior of the nickel silicide nanowires.

Thus, these experiments illustrate that semiconducting silicon nanowires have been successfully transformed into metallic nickel silicide nanowires. Using previously reported carrier density value in nickel silicide the scattering mean free path was estimated to be about 5 nm, which also illustrates that further scaling down of nickel silicide nanowires to sub-10 nm dimensions could be achieved (for example, to 8 nm, 5 nm, 3 nm, or even 1 nm or less) without major changes in performance.

EXAMPLE 5

This example illustrates the transport behavior of nickel silicide nanowires under high electric field conditions by applying bias voltages of up to 2 V to the nanowires. In Fig. 2B, a maximum current of about 1.84 mA was passed through the same nanowire as in Fig. 2A (see Example 4). It was found that the nanowire broke at a bias of about 1.88 V.

Multiple experiments involving nanowire breakdowns illustrated that above a certain low bias, about 1 V in this case, all of the I-V curves observed appeared to become non-linear and showed a decrease in dI/dV (see Fig. 2B). This observation may be accounted for by additional electron-phonon scattering process. Also observed in these experiments was that nearly all of the nanowire breakdowns happened after the nonlinearity turning point. This correlation suggested that the breakdown process may be related to the elevated excitation of high energy optical phonons, and the heat dissipation it brings. SEM results (see, e.g., the inset in Fig. 2B) showed that the nanowire was broken in approximately its middle, which would have a peak temperature caused by dissipative self-heating. The scale bar represents 500 nm in Fig. 2B. This observation

also suggested that the breakdown mechanism may be due to high temperature melting effect.

Using the I-V and diameter data in Fig. 2, the maximum current density, J_{max}, was determined to be about 3×10^8 A/cm^2 for these particular nanowires. However, some nanowires were found to have lost contact with the metal electrodes after high bias, but remained intact after reaching maximum currents as high as 5 mA, suggesting that the current carrying capability can be even higher for certain single-crystal nickel silicide nanowires under optimized conditions, for example, as high as about 10 mA or about 15 mA, or even higher. Moreover, the total amount of current can be scaled up by using NiSi nanowires with larger diameters.

Thus, in summary, the existence of such a high current density may be attributable to the single crystallinity of the nanowires studied. The localized energy dissipation at grain boundary and defect sites would be largely quenched. Also, the absence of grain boundaries suppressed void diffusion paths, thereby resulting in high resistance to electromigration until under extremely high fields.

EXAMPLE 6

In this example, the integration of metallic nickel silicide nanowires into nanoscale devices made by semiconducting silicon nanowires was illustrated. NiSi/Si nanowire heterostructures were fabricated via lithographically defined nickel silicide regions on silicon nanowires, using techniques similar to those discussed in Example 2. In this example, a periodic mask was used to produce a periodic heterostructure in the final nanowire; however, other patterns (including nonperiodic ones) may also be created.

Fig. 3B is a dark field optical image of a single NiSi/Si heterostructured nanowire. The lighter segments 35 correspond to silicon and the dark segments 36 to nickel silicide. The difference in contrast may be attributable to the different reflectivities of the two materials. Control experiments (not shown) using pure silicon nanowires or pure nickel nanowires also showed the same general contrast difference using optical microscopy. The periodic heterostructure extended up to several tens of micrometers over the full length of the nanowire. The scale bar in Fig. 3B is 40 microns.

A typical TEM image of a NiSi/Si heterostructured nanowire is shown in Fig. 3C. The bright segments of the nanowire (average length of about 0.93 microns) corresponded to silicon, while dark segments (average length of about 1.03 microns)

corresponded to nickel silicide. This contrast difference is believed to be due to a larger electron scattering cross section in nickel than in silicon This modulation in axial composition was also confirmed by EDS analysis. The scale bar represents 1 micron.

A HRTEM image of the junction between nickel silicide and silicon (Fig. 3D) showed an atomically abrupt interface. The insets in Fig. 3D illustrate two-dimensional Fourier transforms of the image depicting the [110] and [111] zone axes of NiSi and Si, respectively, with a nickel silicon growth front in the (221) plane and Si growth front in the (112) plane. The scale bar indicates 5 nm.

EXAMPLE 7

In this example, the transport properties of certain NiSi/Si heterostructured nanowires were studied. Field-effect transistor (FET) devices were fabricated using NiSi/p-Si/NiSi nanowire heterostructures similar to those described in Example 6. The source and drain contact regions were fabricated on nickel silicide domains far from the doped silicon channel. Fig. 4A presents typical FET characteristics of such a heterojunction. The linear source-drain current (I_{SD}) vs. bias voltage (V_{SD}) curves suggested that the NiSi/Si contact is approximately ohmic at room temperature, and the changes in I_{SD} at different back-gate voltages (V_G) demonstrated that the p-silicon region functioned as a switching channel. A gate sweep (I_{SD} vs. V_G, inset, Fig. 4A) obtained from the same device at a saturation bias voltage of about -3 V showed that the holes can be depleted at a threshold voltage of about 3.4 V.

Scanning gate microscopy (SGM) images showed reduced conductance at +9 V gate voltage (Fig. 4C) and enhanced conductance at –9 V gate voltage (Fig. 4D) on the atomic force microscopy (AFM) tip. This region is generally confined to the silicon part of the nanowire heterostructure when compared with scanning electron microscopy (SEM) image (Fig. 4B) and dark field optical image (Inset, Fig. 4B). This illustrates that this is a spatially well-defined metal-semiconductor system. The scale bar in both images is 3 microns.

Temperature-dependent transport measurement on a single NiSi/p-Si junction were also performed. It was determined that the effective Shottky barrier height (Φ_B) for holes was about 640 meV, suggesting that the ohmic contacts between nickel silicide and silicon may be due to a "squeezing out" of the dopant atoms toward the interface during formation of nickel silicide thereby forming a highly doped silicon region at the

interface, which reduces the barrier width and promotes direct tunneling current. The scale bars in Fig. 4C and 4D each represent 3 microns.

EXAMPLE 8

This example illustrates the preparation of certain NiSi/Si nanowire heterostructures, according to another embodiment of the invention.

Si nanowires dispersed in ethanol were deposited on a Si wafer with 600 nm thermal oxide, and then the substrate was coated with photoresist (Shipley 1813, Rohm and Haas Electronics Materials LLC, North Andover, MA). The photoresist was exposed for about 2 s on an ABM photoaligner using a simple striped pattern with a 2 micrometer pitch: 1 micrometer line-width and 1 micrometer spacing. After developing for about 1 min, the wafer was transferred to a thermal evaporator and Ni was evaporated with a thickness equal to the average nanowire diameter. Following lift-off, the samples were annealed and etched. Ultrasmall NiSi/Si/NiSi nanowire heterostructures were fabricated using crossed Si/SiO_2 core-shell nanowires using established protocols (see, e.g., Serial No. 10/152,490, entitled, "Nanoscale Wires and Related Devices," filed May 20, 2002) as masks to define the lengths of the unreacted Si regions. The crossed nanowire structures were assembled on Si_3N_4 8 membrane window grids (Structure Probe Inc., West Chester, PA) by fluidic assembly (see, e.g., Serial No. 10/152,490, entitled, "Nanoscale Wires and Related Devices," filed May 20, 2002), and then Ni was evaporated and annealed. The Si/SiO_2 core-shell nanowires were removed with hydrogen fluoride solution (Transene Co., Danvers, MA) to enable direct TEM imaging of the NiSi/Si/NiSi heterostructure on the Si_3N_4 membranes.

Fig. 6A is a schematic illustrating the production of NiSi/Si/NiSi heterostructures. In this figure, on surface 61, Si nanowires 63 are crossed with 3 Si/SiO_2 core/shell nanowires 65. Deposition, annealing and removal of excess Ni yields NiSi regions 67 separated by Si in the nanowire (masked by nanowires 65), as seen on surface 62.

Fig. 6B is a TEM image of a NiSi/Si/NiSi nanowire heterostructure, following removal of the crossed nanowire mask, showing a well-defined silicon channel of 20 nm in this 10 nm diameter NiSi/Si/NiSi heterostructure. The dark regions 68 correspond to NiSi and the light regions 69 to Si, with NiSi/Si interfaces 64 highlighted by black arrows. The scale bar represents 10 nm. The inset shows a TEM image of the same nanowire before silicidation. The crossed Si/SiO_2 core/shell nanowire 66 (approximately

vertical in image) was used as a mask to define the Si region and removed after silicidation. The scale bar in the inset represents 20 nm. The sample was prepared and imaged on a 50 nm thick Si_3N_4 membrane. Additionally, a cross-sectional measurement of the nanowire, as shown in Fig. 6C, shows a relatively sharp boundary between the Si portions and the NiSi portions of the heterostructure.

Figs. 6D-6F shows additional examples, in which Si/SiO_2 core/shell nanowire having other diameters were used as nanowire masks. Fig. 6D shows a Si/SiO_2 core/shell nanowire having a diameter of 148.1 ± 9.4 nm (left) that was used to produce a silicon channel of 134.5 ± 15.8 nm in a NiSi/Si/NiSi heterostructure (right). Similarly, Fig. 6E shows a Si/SiO_2 core/shell nanowire having a diameter of 50.0 ± 3.1 nm (left) used to produce a silicon channel of 38.0 ± 7.3 nm (right), and Fig. 6F shows a Si/SiO_2 core/shell nanowire having a diameter of 19.8 ± 2.0 nm (left) used to produce a silicon channel of about 10 nm (right).

The TEM results indicate lateral diffusion of several nanometers during the formation of NiSi, and shows that it is possible to prepare shorter channel devices in a well-defined manner by varying the diameter of the nanowire mask. More generally, the capability of transforming Si to NiSi in a spatially well-defined manner to form NiSi/Si nanowire heterostructures and superlattices with atomically sharp metal/semiconductor interfaces, opens up the ability of integrating both active devices and high-performance interconnects from a single nanoscale building block. By extending this approach to crossed nanowires, it is possible to assemble large and dense arrays, for example using Langmuir-Blodgett assembly techniques, of transistors and other devices, for example, for use in hybrid integrated circuits, stand-alone integrated nanosystems, or the like.

Of course, the technique illustrated in Figs. 6A and 6B can be applied to any of the embodiments described herein involving introducing one species into another species, such as diffusing at least a portion of a bulk metal into a semiconductor wire.

EXAMPLE 9

This example illustrates the correlation between structure and transport, in various NiSi/Si/NiSi heterostructures, prepared using techniques similar to those described above.

Fig. 7C illustrates current versus voltage, for nickel-contacting silicon nanowires (non-annealed). These wires are shown in Figs. 7A and 7B. Fig. 7D illustrates the formation of a single crystal silicide from a silicon nanowire, at 350 °C, annealed for 5

minutes. Figs. 7E-7G illustrate performance of the Si/NiSi heterostructure after annealing of the nickel to the silicon nanowire to form NiSi. Scale bars in Figs. 7A and 7E represent 1 micron; scale bars in Figs. 7B, 7D, and 7F represent 50 nm.

While several embodiments of the present invention have been described and illustrated herein, those of ordinary skill in the art will readily envision a variety of other means and/or structures for performing the functions and/or obtaining the results and/or one or more of the advantages described herein, and each of such variations and/or modifications is deemed to be within the scope of the present invention. More generally, those skilled in the art will readily appreciate that all parameters, dimensions, materials, and configurations described herein are meant to be exemplary and that the actual parameters, dimensions, materials, and/or configurations will depend upon the specific application or applications for which the teachings of the present invention is/are used. Those skilled in the art will recognize, or be able to ascertain using no more than routine experimentation, many equivalents to the specific embodiments of the invention described herein. It is, therefore, to be understood that the foregoing embodiments are presented by way of example only and that, within the scope of the appended claims and equivalents thereto, the invention may be practiced otherwise than as specifically described and claimed. The present invention is directed to each individual feature, system, article, material, kit, and/or method described herein. In addition, any combination of two or more such features, systems, articles, materials, kits, and/or methods, if such features, systems, articles, materials, kits, and/or methods are not mutually inconsistent, is included within the scope of the present invention.

All definitions, as defined and used herein, should be understood to control over dictionary definitions, definitions in documents incorporated by reference, and/or ordinary meanings of the defined terms.

The phrase "and/or," as used herein in the specification and in the claims, should be understood to mean "either or both" of the elements so conjoined, i.e., elements that are conjunctively present in some cases and disjunctively present in other cases. Other elements may optionally be present other than the elements specifically identified by the "and/or" clause, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, a reference to "A and/or B", when used in conjunction with open-ended language such as "comprising" can refer, in one embodiment, to A only

(optionally including elements other than B); in another embodiment, to B only (optionally including elements other than A); in yet another embodiment, to both A and B (optionally including other elements); etc.

As used herein in the specification and in the claims, the phrase "at least one," in reference to a list of one or more elements, should be understood to mean at least one element selected from any one or more of the elements in the list of elements, but not necessarily including at least one of each and every element specifically listed within the list of elements and not excluding any combinations of elements in the list of elements. This definition also allows that elements may optionally be present other than the elements specifically identified within the list of elements to which the phrase "at least one" refers, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, "at least one of A and B" (or, equivalently, "at least one of A or B," or, equivalently "at least one of A and/or B") can refer, in one embodiment, to at least one, optionally including more than one, A, with no B present (and optionally including elements other than B); in another embodiment, to at least one, optionally including more than one, B, with no A present (and optionally including elements other than A); in yet another embodiment, to at least one, optionally including more than one, A, and at least one, optionally including more than one, B (and optionally including other elements); etc.

It should also be understood that, unless clearly indicated to the contrary, in any methods claimed herein that include more than one act, the order of the acts of the method is not necessarily limited to the order in which the acts of the method are recited.

In the claims, as well as in the specification above, all transitional phrases such as "comprising," "including," "carrying," "having," "containing," "involving," "holding," and the like are to be understood to be open-ended, i.e., to mean including but not limited to. Only the transitional phrases "consisting of" and "consisting essentially of" shall be closed or semi-closed transitional phrases, respectively, as set forth in the United States Patent Office Manual of Patent Examining Procedures, Section 2111.03.

What is claimed is:

CLAIMS

1. A method, comprising:

providing a bulk metal adjacent a semiconductor wire; and

diffusing at least a portion of the bulk metal into at least a portion of the semiconductor wire, the semiconductor wire comprising at least one portion having a smallest dimension of less than about 500 nm.

2. The method of claim 1, wherein the bulk metal comprises a transition metal.

3. The method of claim 2, wherein the transition metal includes at least one of a Group IIIB element, a Group IVB element, a Group VB element, a Group VIB element, a Group VIIB element, and a Group VIIIB element.

4. The method of claim 3, wherein the bulk metal comprises a Group VIIIB element.

5. The method of claim 1, wherein the bulk metal comprises nickel.

6. The method of claim 1, wherein the bulk metal consists essentially of nickel.

7. The method of claim 1, wherein the semiconductor comprises an elemental semiconductor.

8. The method of claim 7, wherein the elemental semiconductor comprises at least one of silicon, gallium, germanium, carbon, tin, selenium, tellurium, boron, or phosphorous.

9. The method of claim 7, wherein the elemental semiconductor comprises a Group IV semiconductor.

10. The method of claim 7, wherein the elemental semiconductor comprises Si.

11. The method of claim 7, wherein the elemental semiconductor consists essentially of Si.

12. The method of claim 1, wherein the smallest dimension is less than 200 nm.

13. The method of claim 1, wherein the smallest dimension is less than 150 nm.

14. The method of claim 1, wherein the smallest dimension is less than 100 nm.

15. The method of claim 1, wherein the smallest dimension is less than 80 nm.

16. The method of claim 1, wherein the smallest dimension is less than 70 nm.

17. The method of claim 1, wherein the smallest dimension is less than 60 nm.

18. The method of claim 1, wherein the smallest dimension is less than 40 nm.

19. The method of claim 1, wherein the smallest dimension is less than 20 nm.

20. The method of claim 1, wherein the smallest dimension is less than 10 nm.

21. The method of claim 1, wherein the smallest dimension is less than 5 nm.

22. The method of claim 1, wherein the wire has an aspect ratio of at least 4:1.

23. The method of claim 1, wherein the wire has an aspect ratio of at least 10:1.

24. The method of claim 1, wherein the wire has an aspect ratio of at least 100:1.

25. The method of claim 1, wherein the wire has an aspect ratio of at least 1000:1.

26. The method of claim 1, wherein the wire is a single crystal.

27. An article, comprising:

a wire comprising at least one metal silicide, the wire being a single crystal.

28. The article of claim 27, wherein the metal comprises a transition metal.

29. The article of claim 28, wherein the transition metal includes at least one of a Group IIIB element, a Group IVB element, a Group VB element, a Group VIB element, a Group VIIB element, and a Group VIIIB element.

30. The article of claim 29, wherein the metal is a Group VIIIB element.

31. The article of claim 30, wherein the metal comprises nickel.

32. The article of claim 27, wherein the wire comprises at least one portion having a smallest dimension of less than about 500 nm.

33. The article of claim 27, wherein the wire has an aspect ratio of at least 4:1.

34. The article of claim 27, wherein the wire is part of a device.

35. The article of claim 34, wherein the device is an electronic device.

36. The article of claim 34, wherein the device is a switch.

37. The article of claim 34, wherein the device is a logic unit.

38. The article of claim 34, wherein the device is a transistor.

39. The article of claim 38, wherein the transistor is a field effect transistor.

40. The article of claim 34, wherein the device comprises a digital circuit.

41. The article of claim 27, wherein the metal silicide comprises a stoichiometric ratio of silicon and at least one metal.

42. The article of claim 27, wherein the wire has a resistivity of less than about 60 microOhm cm.

43. The article of claim 27, wherein the wire is able to carry a current density of at least about 10^8 A/cm^2.

44. An article, comprising:

a wire comprising a compound having a stoichiometric ratio of silicon and at least one metal, the wire comprising at least one portion having a smallest dimension of less than about 500 nm.

45. The article of claim 44, wherein the metal comprises a transition metal.

46. The article of claim 45, wherein the transition metal comprises nickel.

47. The article of claim 44, wherein the wire comprises at least one portion having a smallest dimension of less than about 500 nm.

48. The article of claim 44, wherein the wire has an aspect ratio of at least 4:1.

49. The article of claim 44, wherein the wire is part of a device.

50. The article of claim 44, wherein the wire is a single crystal.

51. The article of claim 44, wherein the wire has a resistivity of less than about 60 microOhm cm.

52. The article of claim 44, wherein the wire is able to carry a current density of at least about 10^8 A/cm^2.

53. The article of claim 44, wherein the wire comprises two regions differing in composition, at least one of the two regions comprising the compound having the stoichiometric ratio of silicon and at least one metal.

54. An article, comprising:

a wire comprising at least one metal silicide, the wire having a resistivity of less than about 60 microOhm cm.

55. The article of claim 54, wherein the metal comprises a transition metal.

56. The article of claim 55, wherein the metal comprises nickel.

57. The article of claim 54, wherein the wire comprises at least one portion having a smallest dimension of less than about 500 nm.

58. The article of claim 54, wherein the wire has an aspect ratio of at least 4:1.

59. The article of claim 54, wherein the wire is part of a device.

60. The article of claim 54, wherein the wire is a single crystal.

61. The article of claim 54, wherein the metal silicide comprises a stoichiometric ratio of silicon and at least one metal.

62. The article of claim 54, wherein the wire is able to carry a current density of at least about 10^8 A/cm^2.

63. The article of claim 54, wherein the wire comprises two regions differing in composition, at least one of the two regions comprising the metal silicide.

64. An article, comprising:

a wire comprising at least one metal silicide, the wire being able to carry a current density of at least about 10^8 A/cm^2.

65. The article of claim 64, wherein the metal comprises a transition metal.

66. The article of claim 65, wherein the metal comprises nickel.

67. The article of claim 64, wherein the wire comprises at least one portion having a smallest dimension of less than about 500 nm.

68. The article of claim 64, wherein the wire has an aspect ratio of at least 4:1.

69. The article of claim 64, wherein the wire is part of a device.

70. The article of claim 64, wherein the wire is a single crystal.

71. The article of claim 64, wherein the metal silicide comprises a stoichiometric ratio of silicon and at least one metal.

72. The article of claim 64, wherein the wire has a resistivity of less than about 60 microOhm cm.

73. The article of claim 64, wherein the wire comprises two regions differing in composition, at least one of the two regions comprising the metal silicide.

74. An article, comprising:

a wire comprising at least two regions differing in composition, at least one region comprising a metal silicide, the wire comprising at least one portion having a smallest dimension of less than about 500 nm.

75. The article of claim 74, wherein the metal comprises a transition metal.

76. The article of claim 75, wherein the metal comprises nickel.

77. The article of claim 74, wherein the wire has an aspect ratio of at least 4:1.

78. The article of claim 74, wherein the wire is part of a device.

79. The article of claim 74, wherein the metal silicide comprises a stoichiometric ratio of silicon and at least one metal.

80. The article of claim 74, wherein the wire has a resistivity of less than about 60 microohm cm.

81. The article of claim 74, wherein the wire is able to carry a current density of at least about 10^8 A/cm^2.

82. The article of claim 74, wherein each of the at least two regions independently comprises a metal silicide.

83. The article of claim 74, wherein two of the at least two regions define a boundary therebetween, the boundary being atomically abrupt.

84. The article of claim 74, the at least two regions comprising a first region having a composition and a second region having a composition different from the first region, the first region and the second region overlapping to form an overlap region having a composition that is a mixture of the compositions of the first and second regions, wherein the composition of the overlap region comprises between about 10 vol% and about 90 vol% of the composition of the first region with a complementary amount of the composition of the second region.

85. An article, comprising:

a wire comprising at least two regions differing in composition and a boundary between the at least two regions, the boundary having a maximum dimension of less than about 500 nm, wherein at least one region comprises a metal silicide.

86. The article of claim 85, wherein the metal comprises a transition metal.

87. The article of claim 86, wherein the metal comprises nickel.

88. The article of claim 85, wherein the wire has an aspect ratio of at least 4:1.

89. The article of claim 85, wherein the wire is part of a device.

90. The article of claim 85, wherein the metal silicide comprises a stoichiometric ratio of silicon and at least one metal.

91. The article of claim 85, wherein the wire has a resistivity of less than about 60 microOhm cm.

92. The article of claim 85, wherein the wire is able to carry a current density of at least about 10^8 A/cm^2.

93. The article of claim 85, wherein the maximum dimension is less than 200 nm.

94. The article of claim 85, wherein the boundary is an atomically abrupt boundary.

95. The article of claim 85, wherein the at least two regions each independently comprises a metal silicide.

96. A method, comprising:

diffusing a material into at least a portion of a wire, the wire comprising at least one portion having a smallest dimension of less than about 500 nm.

97. The method of claim 96, wherein the material comprises a metal.

98. The method of claim 97, wherein the metal comprises nickel.

99. The method of claim 96, wherein the wire comprises a semiconductor.

100. The method of claim 99, wherein the semiconductor comprises silicon.

101. The method of claim 96, comprising diffusing the first material into a first portion of a wire without diffusing the first material into a second portion of the wire.

102. The method of claim 101, wherein the first portion and the second portion of the wire are defined by a mask positioned proximate the wire.

103. The method of claim 102, wherein the mask comprises photoresist.

104. The method of claim 102, wherein the mask comprises a nanoscale wire.

105. The method of claim 104, wherein the nanoscale wire comprises a core and a shell.

106. The method of claim 104, further comprising positioning a mask proximate the semiconductor, the mask defining, at least in part, the portion of the semiconductor that at least a portion of the bulk metal diffuses into.

107. The method of claim 106, wherein the mask comprises photoresist.

108. The method of claim 106, wherein the mask comprises a nanoscale wire.

109. The method of claim 108, wherein the nanoscale wire comprises a core and a shell.

110. A method, comprising:

diffusing a metal into at least a portion of a semiconductor nanoscale wire to form a stoichiometric ratio of metal atoms to semiconductor atoms within the portion of the semiconductor nanoscale wire.

111. The method of claim 110, wherein the metal comprises a transition metal.

112. The method of claim 110, wherein the metal comprises nickel.

113. The method of claim 110, wherein the metal consists essentially of nickel.

114. The method of claim 110, wherein the semiconductor comprises an elemental semiconductor.

115. The method of claim 110, wherein the elemental semiconductor comprises Si.

116. The method of claim 110, wherein the elemental semiconductor consists essentially of Si.

117. A method, comprising:

bulk-doping at least a portion of a nanoscale wire after growth of the nanoscale wire.

118. The method of claim 117, wherein bulk-doping comprises doping a center portion of the nanoscale wire.

119. The method of claim 117, comprising bulk-doping the nanoscale wire to increase the conductivity of the nanoscale wire.

120. The method of claim 117, comprising diffusing a metal into at least a portion of the semiconductor nanoscale wire.

121. A method, comprising:

diffusing a material into a center portion of a semiconductor wire, the semiconductor wire comprising at least one portion having a smallest dimension of less than about 500 nm.

122. The method of claim 121, comprising diffusing at least a portion of the material to alter the conductivity of the portion of the semiconductor wire.

123. The method of claim 121, wherein the material comprises a metal.

124. The method of claim 123, wherein the metal comprises a transition metal.

125. The method of claim 123, wherein the metal comprises nickel.

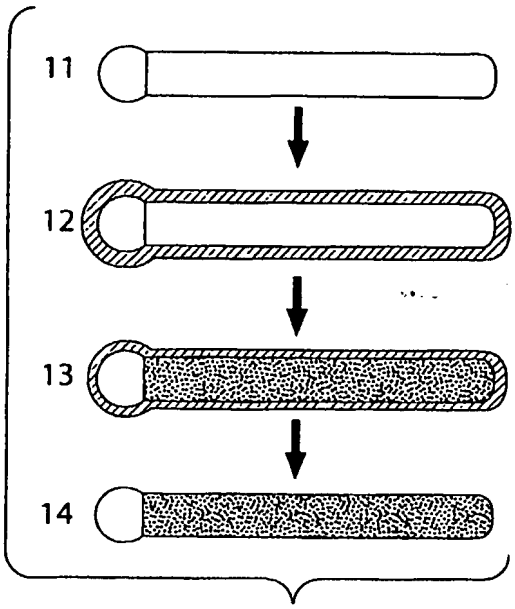

Fig. 1A

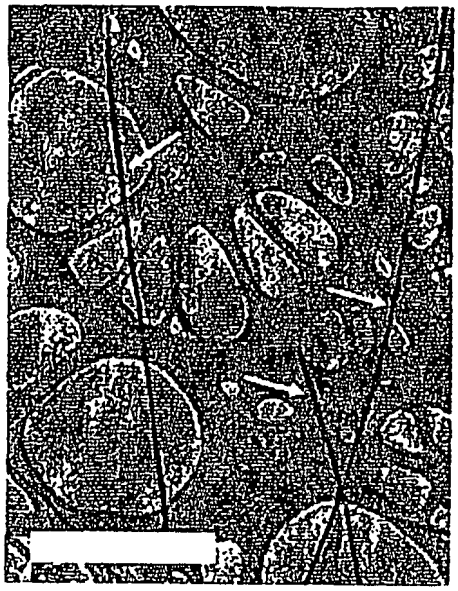

Fig. 1B

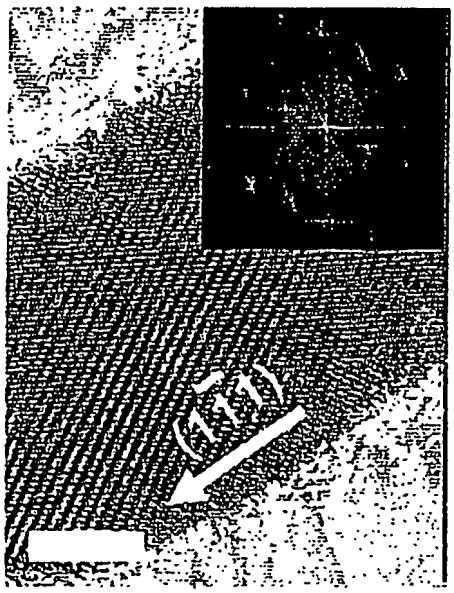

Fig. 1C

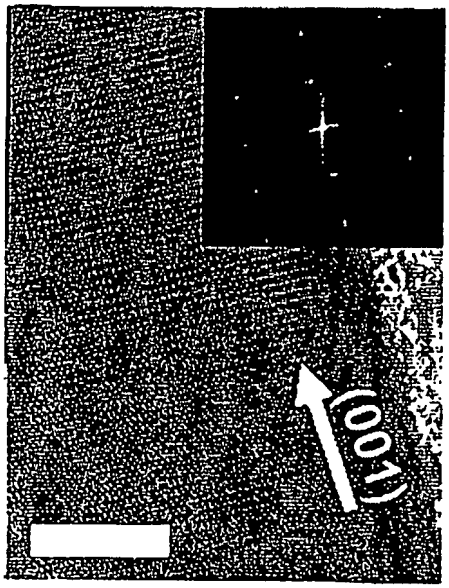

Fig. 1D

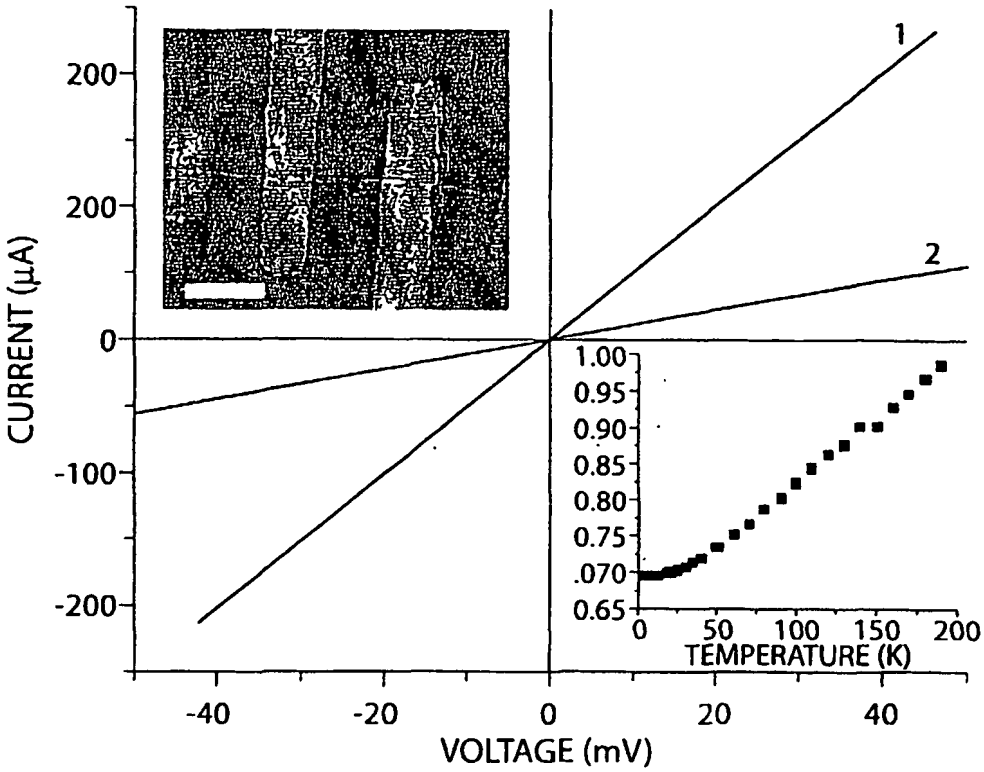
200
200
0
-100
-200
CURRENT (μA)
1
2
-40
-20
0
20
40
VOLTAGE (mV)
1.00
0.95
0.90
0.85
0.80
0.75
.070
0.65
0
50
100
150
200
TEMPERATURE (K)

Fig. 2A

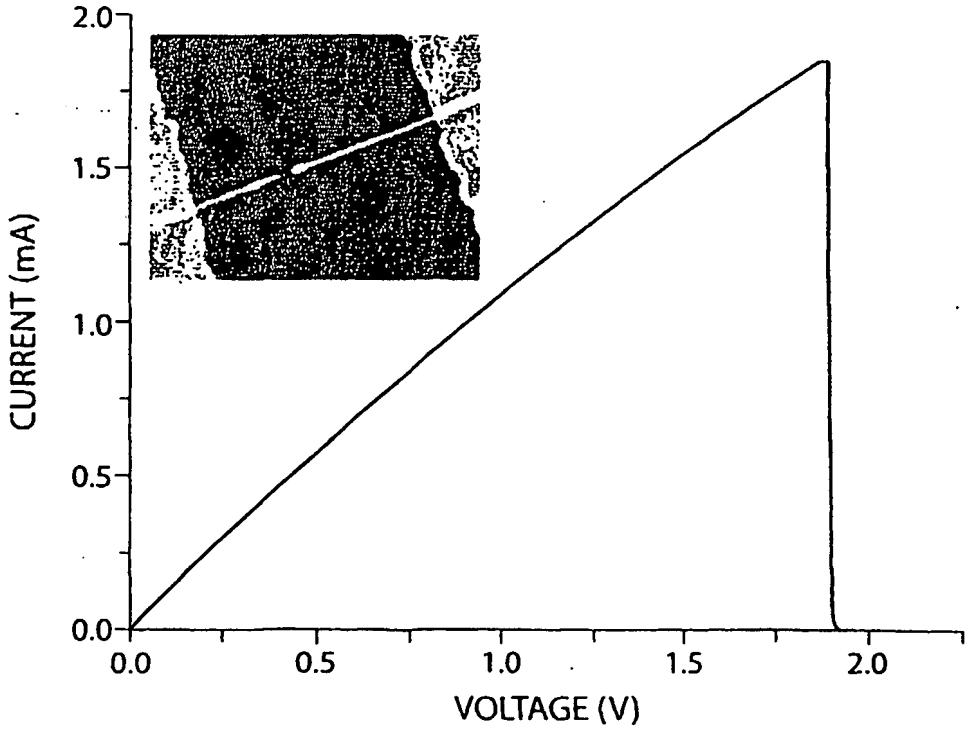
2.0
1.5
1.0
0.5
0.0
CURRENT (mA)
0.0
0.5
1.0
1.5
2.0
VOLTAGE (V)

Fig. 2B

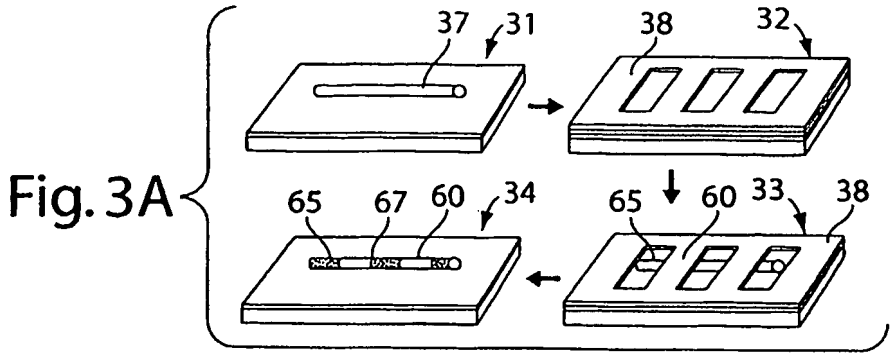

Fig. 3A

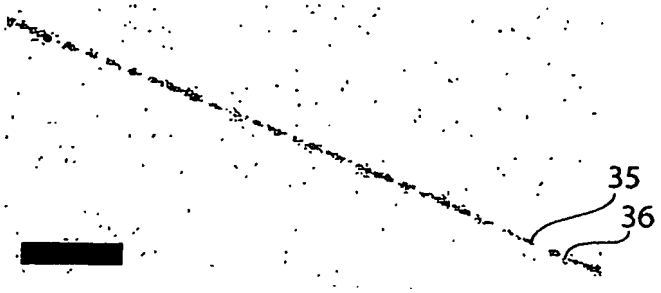

Fig. 3B

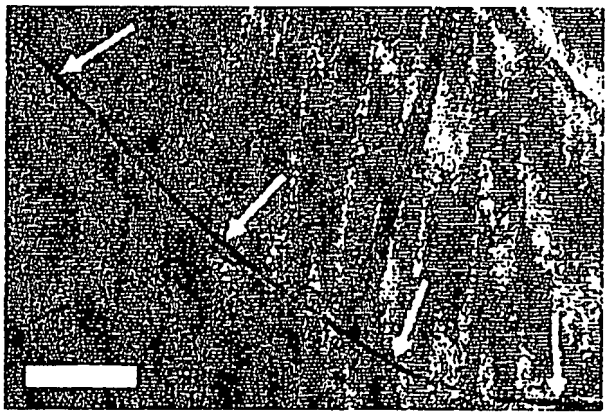

Fig. 3C

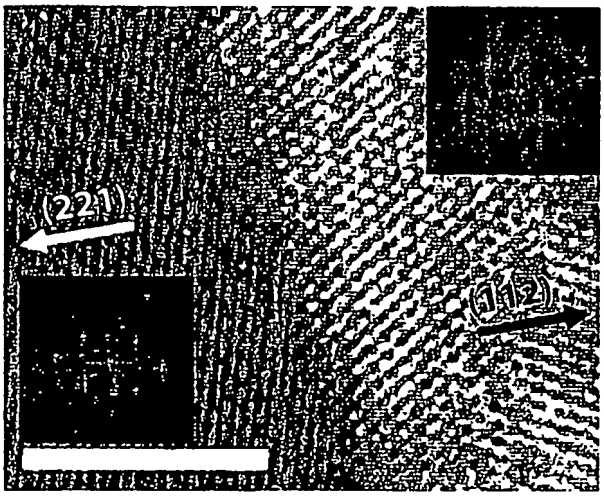

Fig. 3D

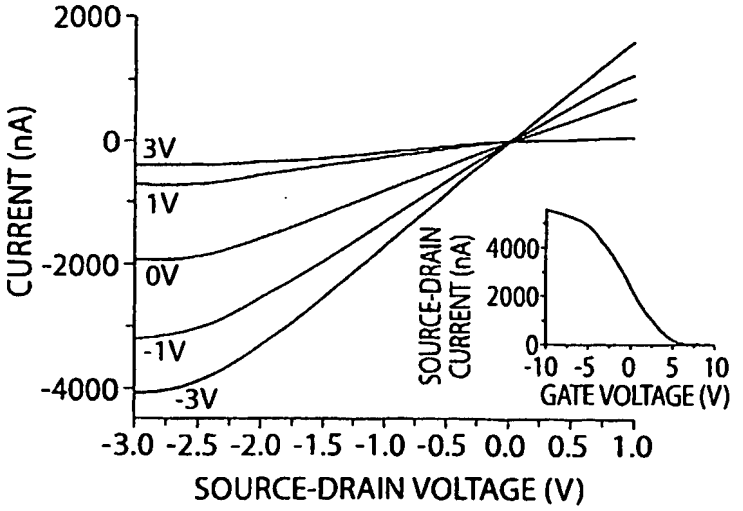

Fig. 4A

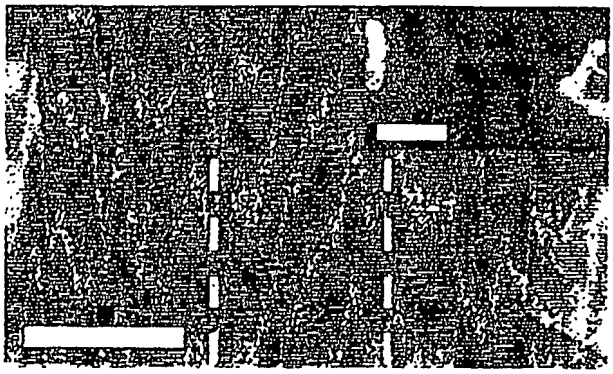

Fig. 4B

Fig. 4C

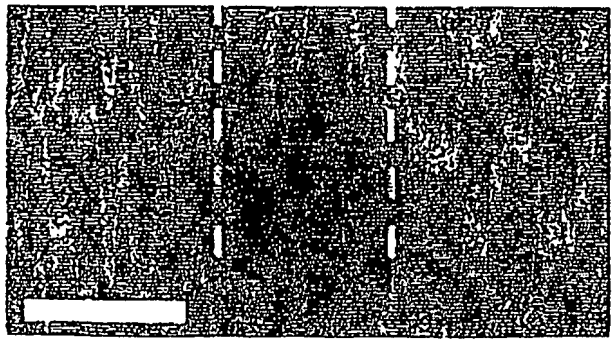

Fig. 4D

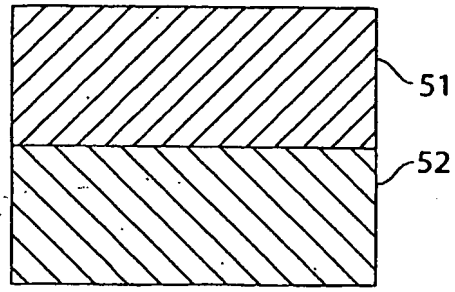

Fig. 5A

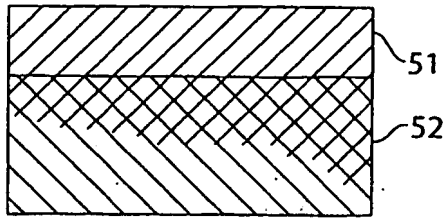

Fig. 5B

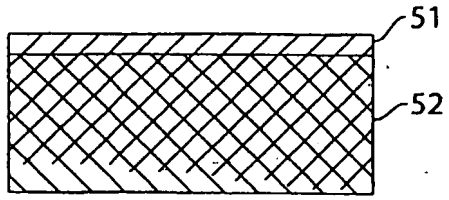

Fig. 5C

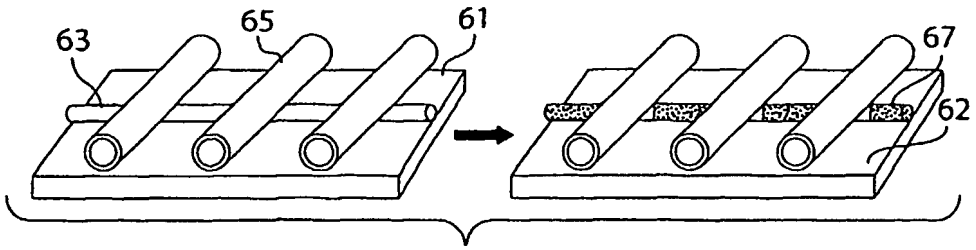

Fig. 6A

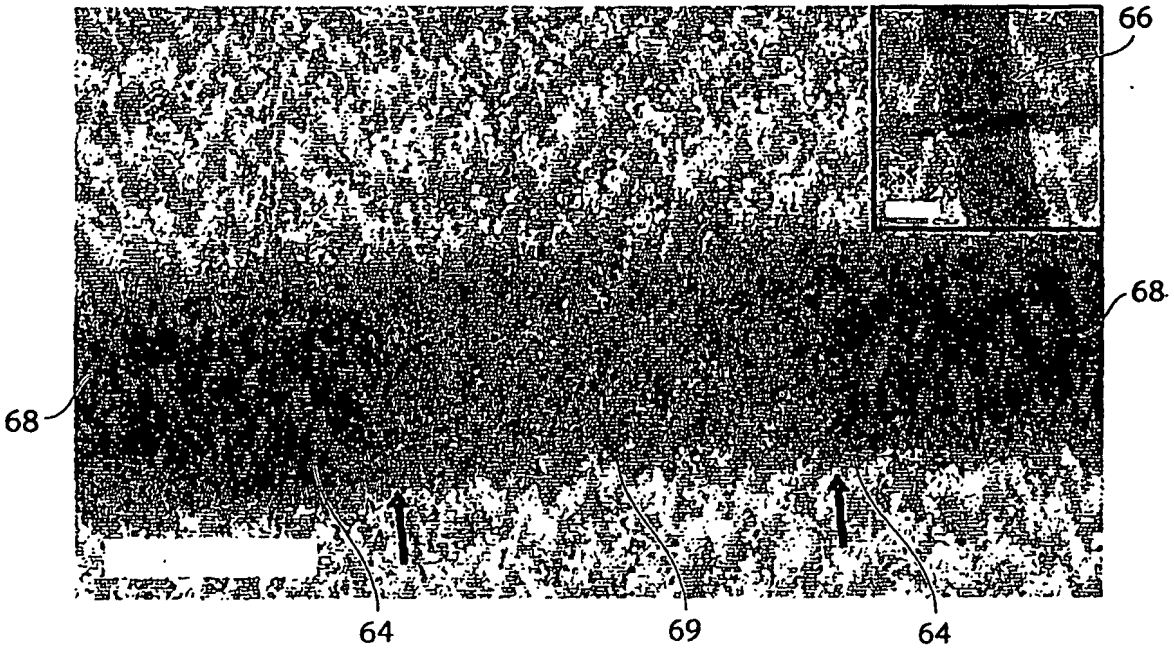

Fig. 6B

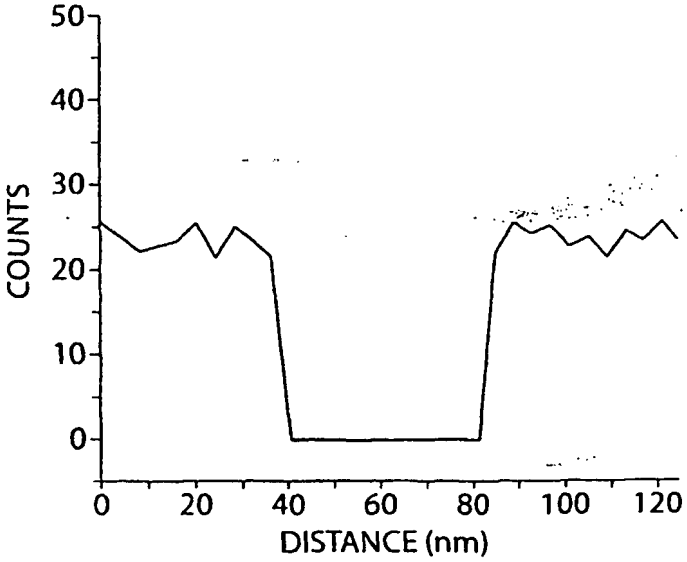

Fig. 6C

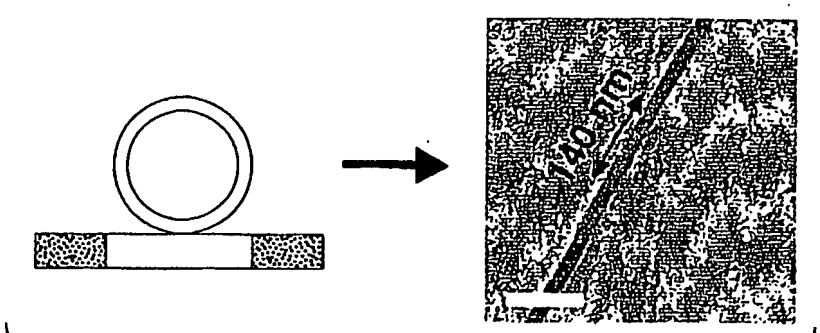

Fig. 6D

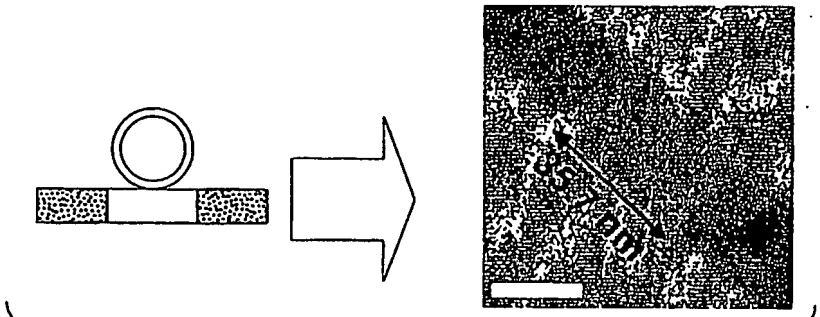

Fig. 6E

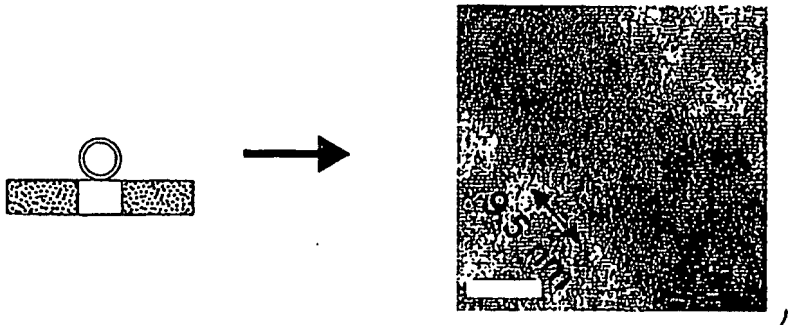

Fig. 6F

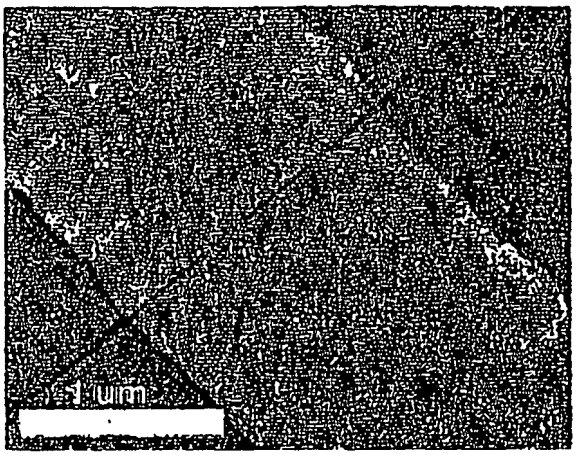

Fig. 7A

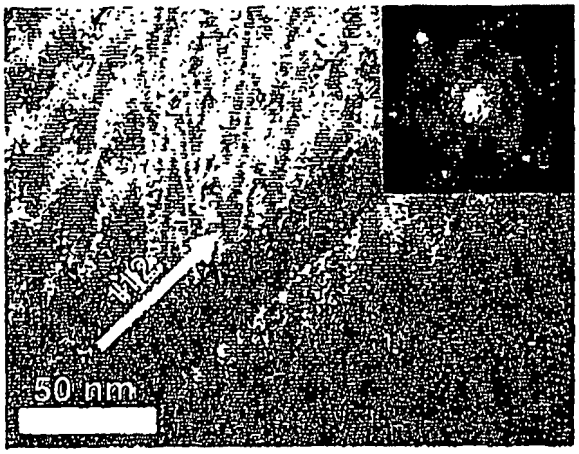

Fig. 7B

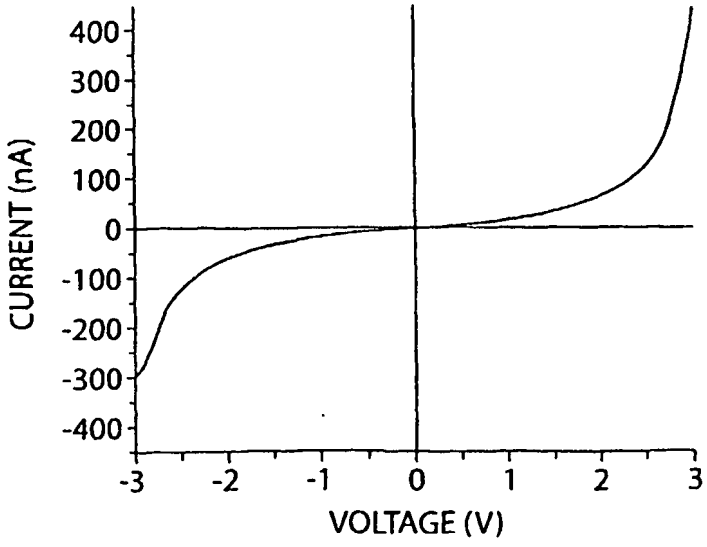

Fig. 7C

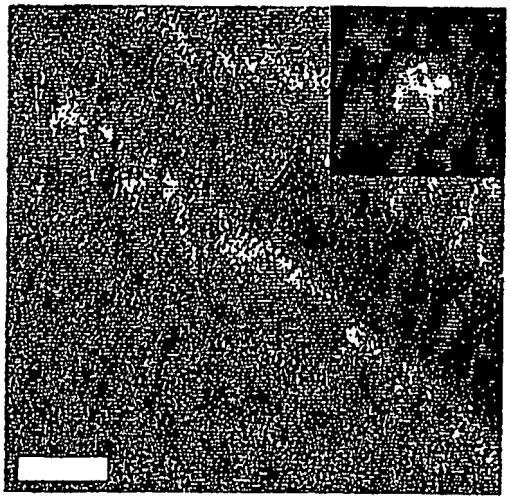

Fig. 7D

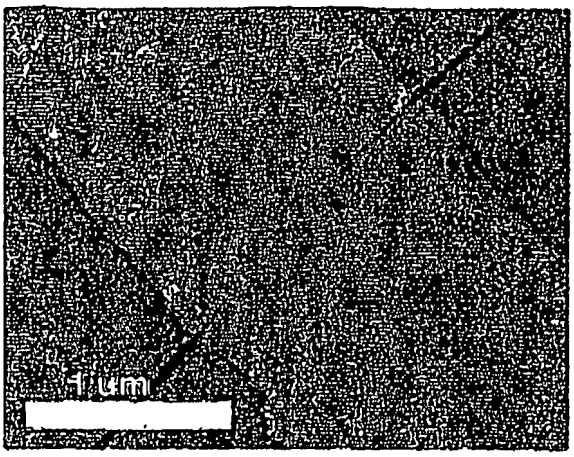

Fig. 7E

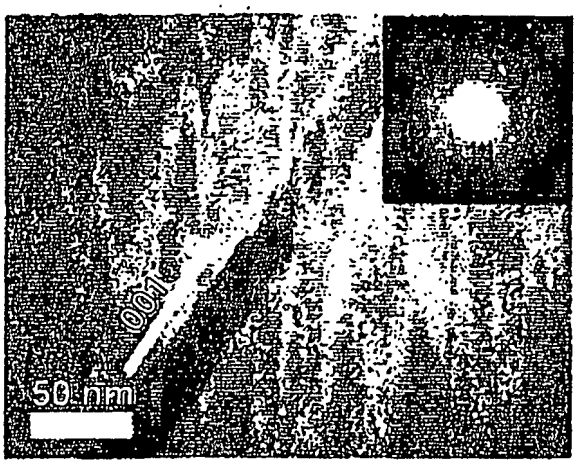

Fig. 7F

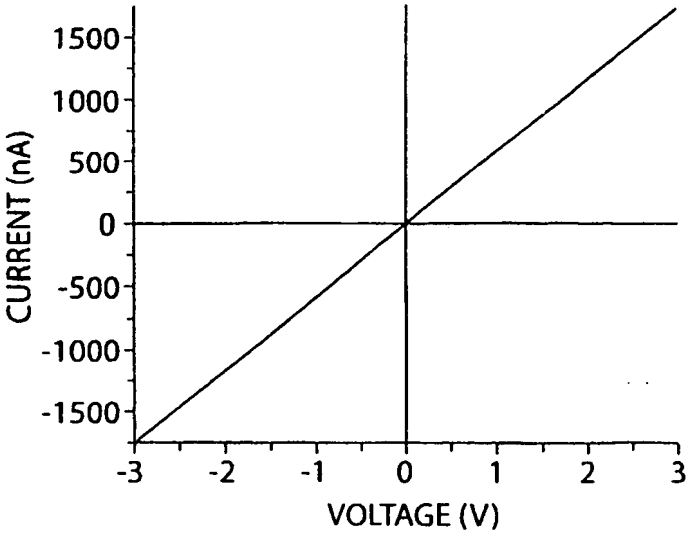

Fig. 7G

INTERNATIONAL SEARCH REPORT

Inte I Application No
PCT/US2005/004459

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L23/49

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2004/003535 A (NANOSYS INC; PONTIS, GEORGE; STONAS, WALTER; CHOW, CALVIN; PARCE, WALL) 8 January 2004 (2004-01-08) the whole document	1-26
A	US 2003/186522 A1 (DUAN XIANGFENG ET AL) 2 October 2003 (2003-10-02) paragraph '0082!	

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 August 2005	29/08/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Boetticher, H

Form PCT/ISA/210 (second sheet) (January 2004)

INTERNATIONAL SEARCH REPORT

ıational application No.
PCT/US2005/004459

Box II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 27-125
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

see FURTHER INFORMATION sheet PCT/ISA/210

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box II.2

Claims Nos.: 27-125

Contrary to Article 6 PCT, the claims as a whole are not concise because of 6 independent device claims and 5 independent method claims. Further, due to the various features claimed in the various independent claims it is obscure which features are essential to the invention. For example, the first independent method claim, claim 1, contains the feature that the semiconductor wire comprises at least one portion having a smallest dimension of less than about 500 nm, a feature not contained in the first independent device claim, claim 27, which claim however contains the feature that the wire is a single crystal, a feature not contained in claim 1. Further, the term "wire" used both in claim 1 and in claim 27 is so broad that it renders D1: WO 2004/003535 A1 - concerning a nanowire formed by etching - novelty destroying to claim 1. Thus, for example, claims 1 and 27 are no longer linked by a single general inventive concept in the sense of Rule 13.1 PCT, and further search fees could be asked for. But asking for further search fees for claims which simply lack unity because they do not show all features essential to the invention seems not appropriate. However, as pointed out above, it is obscure which features are essential to the invention. Since a meaningful search involving a meaningful objection as to lack of unity was not possible, the search is incomplete.

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guideline C-VI, 8.5), should the problems which led to the Article 17(2) declaration be overcome.

INTERNATIONAL SEARCH REPORT

ormation on patent family members

Inte pnal Application No
PCT/US2005/004459

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2004003535 A	08-01-2004	AU 2003258969 A1	19-01-2004
		WO 2004003535 A1	08-01-2004
		US 2004136866 A1	15-07-2004
US 2003186522 A1	02-10-2003	AU 2003222134 A1	20-10-2003
		AU 2003260527 A1	20-10-2003
		EP 1522106 A2	13-04-2005
		EP 1508161 A2	23-02-2005
		WO 03085700 A2	16-10-2003
		WO 03085701 A2	16-10-2003
		US 2004005723 A1	08-01-2004